570232-004

National Semiconductor

Jan.94 Edition

SO-8

DMOS

MOSFETs

National Semiconductor

January 1994

Discrete Products

SO-8 Single and Dual DMOS FET Selection Guide

Part Number	V ds (V)	rDS(on) Ohm Vgs = 10V	rDS(on) Ohm Vgs = 4.5V	ID (A)	Configuration	Sample	Production
N-Channel MOSFETs							
NDS9410	30	0.03	0.05	7	Single	Now	Now
NDS9936	30	0.05	0.08	5	Dual	Now	Now
NDS9945	60	0.1	0.2	3.5	Dual	Now	Now
NDS9955	50	0.13	0.2	3	Dual	Now	Now
NDS9956	20	0.1	0.2	3.5	Dual	Now	Now
P-Channel MOSFETs							
NDS9400	-20	0.25	0.4	-2.5	Single	Now	Now
NDS9405	-20	0.1	0.16	-4.3	Single	Now	Now
NDS9407	-60	0.15	0.24	-3.3	Single	TBD	TBD
NDS9430	-20	0.06	0.115	-5.3	Single	Now	Now
NDS9435	-30	0.07	0.13	-5.3	Single	Now	Now
NDS9947	-20	0.1	0.19	-3.5	Dual	* Q1 '94	* Q2 '94
NDS9948	-60	0.25	0.5	-2.3	Dual	TBD	TBD
NDS9953	-20	0.25	0.4	-2.3	Dual	Now	Now
Complemetary N-P Dual MOSFETs							
NDS9942	20	0.125	0.25	3	N-Channel	Now	Now
	-20	0.2	0.35	-2.5	P-Channel		
NDS9943	20	0.125	0.25	3	N-Channel	* Q1 '94	* Q2 '94
	-20	0.16	0.3	-2.8	P-Channel		
NDS9952	25	0.1	0.15	3	N-Channel	Now	Now
	-25	0.25	0.4	-2.3	P-Channel		
NDS9958	20	0.1	0.15	3.5	N-Channel	* Q1 '94	* Q2 '94
	-20	0.1	0.19	-3	P-Channel		

*Remark:
Target schedule release at the time of publication, actual schedule may change.
Please contact Discrete Marketing for most update status.

Part Number	V ds (V)	rDS(on) Ohm Vgs = 10V	rDS(on) Ohm Vgs = 4.5V	ID (A)	Configuration	Replace the following devices in certain applications
N-Channel MOSFETs						
NDS9410	30	0.03	0.05	7	Single	Si9410DY, MTP50N05, MTP50N05EL
NDS9936	30	0.05	0.08	5	Dual	Si9936DY
NDS9945	60	0.1	0.2	3.5	Dual	Si9945DY, IRFD020, IRFR020, MTD3055E
NDS9955	50	0.13	0.2	3	Dual	Si9955DY, IRFD010, IRFD020, IRFR010, IRFR012, IRFR020, IRFR022, MTD5N05, MTD10N05E
NDS9956	20	0.1	0.2	3.5	Dual	Si9956DY, IRFD010, IRFD022, IRFR020, IRFR022, MTD10N05E, MTD3055E, RFD10N05SM, RFD14N05SM
P-Channel MOSFETs						
NDS9400	-20	0.25	0.4	-2.5	Single	Si9400DY, IRFD9010, IRFD9020, IRFD9120, IRFD9123, IRFR9010, IRFR9020, MTD4P05, MTD2955
NDS9405	-20	0.1	0.16	-4.3	Single	Si9405DY
NDS9407	-60	0.15	0.24	-3.3	Single	Si9407DY, IRFD9010, IRFD9020, IRFD9014, IRFD9024, IRFR9010, IRFR9020, IRFR9014, IRFR9024
NDS9430	-20	0.06	0.115	-5.3	Single	Si9430DY
NDS9435	-30	0.07	0.13	-5.3	Single	Si9435DY
NDS9947	-20	0.11	0.19	-3.5	Dual	Si9947DY, IRFD9010, IRFD9020, IRFD9014, IRFD9024, IRFR9010, IRFR9020, IRFR9014, IRFR9024
NDS9948	-60	0.25	0.5	-2.3	Dual	Si9948DY, IRFD9010, IRFD9020, IRFD9014, IRFD9024, IRFR9010, IRFR9014, IRFR9020, IRFR9024, MTD2955
NDS9953	-20	0.25	0.4	-2.3	Dual	Si9953DY, IRFD9010, IRFD9020, IRFD9120, IRFD9123, IRFR9010, IRFR9020, MTD4P05, MTD2955
Complemetary N-P Dual MOSFETs						
NDS9942	20	0.125	0.25	3	N-Channel	Complementary SO-8s replace following pairs: Si9942DY, Si9943DY, Si9952DY, Si9958DY; (IRFD010, IRFD9010); (IRFD020, IRFD9020); (IRFD110, IRFD9022); (IRFD123, IRFD9123); (IRFR010, IRFR9010); (IRFR020, IRFR9020); (MTD5N05, MTD4P05); (MTD10N05E, MTD2955); (MTD3055E, MTD2955)
	-20	0.2	0.35	-2.5	P-Channel	
NDS9943	20	0.125	0.25	3	N-Channel	
	-20	0.16	0.3	-2.8	P-Channel	
NDS9952	25	0.1	0.15	3	N-Channel	
	-25	0.25	0.4	-2.3	P-Channel	
NDS9958	20	0.1	0.15	3.5	N-Channel	
	-20	0.11	0.19	-3	P-Channel	

National Semiconductor

November 1993

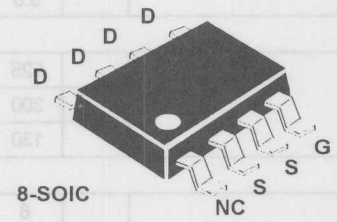
NDS9400
Single P-Channel Enhancement Mode Field Effect Transistor

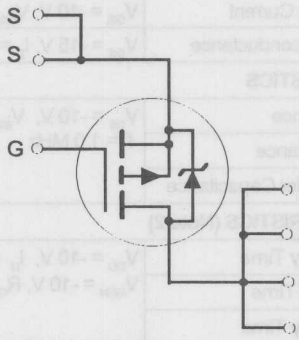
General Description

These P-channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulses in the avalanche and commutation modes. These devices are particularly suited for low voltage applications such as laptop computer power management and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- 2.5A, -20V. $R_{DS(ON)}$ = 0.25Ω.
- Rugged internal source-drain diode can eliminate the need for an external Zener diode transient suppressor.
- High density cell design (3.8 million/in²) for extremely low $R_{DS(ON)}$.
- High power and current handling capability in a widely used surface mount package.
- Critical DC electrical parameters specified at elevated temperature.





Absolute Maximum Ratings

T_c = 25°C unless otherwise noted

Symbol	Parameter		NDS9400	Units
V_{DSS}	Drain-Source Voltage		-20	V
V_{DGR}	Drain-Gate Voltage ($R_{GS} \leq 1$ MΩ)		-20	V
V_{GSS}	Gate-Source Voltage		± 20	V
I_D	Drain Current - Continuous	T_A = 25°C	± 2.5	A
	- Pulsed		± 10	A
	- Continuous	T_A = 70°C	± 2.0	A
P_D	Maximum Power Dissipation	T_A = 25°C	2.5 (Note 1)	W
		T_A = 70°C	1.6 (Note 1)	W
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to 150	°C
THERMAL CHARACTERISTICS				
$R_{\theta JA}(t)$	Thermal Resistance, Junction-to-Ambient (Surface Mounted. Pulse time = 10 seconds)		50 (Note 1)	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Surface Mounted. Steady-State)		100	°C/W

Electrical Characteristics (T_c = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = -250 µA	-20			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -16 V, V_{GS} = 0 V			-2	µA
		T_c = 55°C			-25	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = -250 µA	-1	-2	-3	V
		T_c=125°C	-0.85	-1.7	-2.6	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = -10 V, I_D = -1A		0.18	0.25	Ω
		T_c=125°C		0.24	0.35	Ω
		V_{GS} = -4.5 V, I_D = -0.5 A		0.26	0.4	Ω
		T_c=125°C		0.35	0.56	Ω
$I_{D(on)}$	On-State Drain Current	V_{GS} = -10 V, V_{DS} = -5 V	-10			A
g_{FS}	Forward Transconductance	V_{DS} = -15 V, I_D = -2.5 A		3.8		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = -10 V, V_{GS} = 0 V, f = 1.0 MHz		525		pF
C_{oss}	Output Capacitance			300		pF
C_{rss}	Reverse Transfer Capacitance			130		pF
SWITCHING CHARACTERISTICS (Note 2)						
$t_{D(ON)}$	Turn - On Delay Time	V_{DD} = -10 V, I_D = -1 A, V_{GEN} = -10 V, R_{GEN} = 6 Ω		8	40	ns
t_r	Turn - On Rise Time			15	40	ns
$t_{D(OFF)}$	Turn - Off Delay Time			25	90	ns
t_f	Turn - Off Fall Time			8	50	ns
Q_g	Total Gate Charge	V_{DS} = -10 V, I_D = -2.0 A, V_{GS} = -10 V		15	25	nC
Q_{gs}	Gate-Source Charge			1.2		nC
Q_{gd}	Gate-Drain Charge			4.8		nC
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain-Source Diode Forward Current				-2	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = -1.25 A (Note 2)		-0.94	-1.6	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0V, I_S = 2.0 A, dI_S/dt = 100 A/µs		29	100	ns
I_{rr}	Reverse Recovery Current			1.9		A

Notes:

1. Power dissipation and thermal resistance determinations based on an assumption that a 10 second pulse is equivalent to steady-state.
2. Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

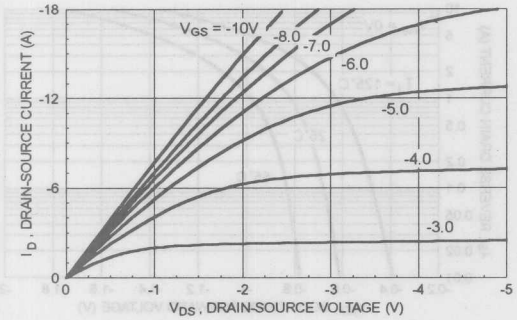


Figure 1. On-Region Characteristics.

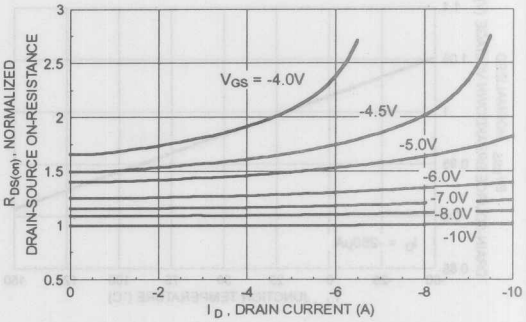


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current.

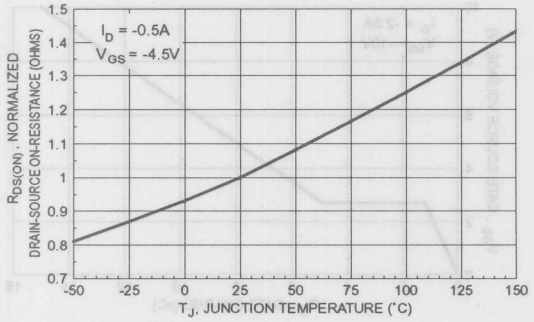


Figure 3. On-Resistance Variation with Temperature.

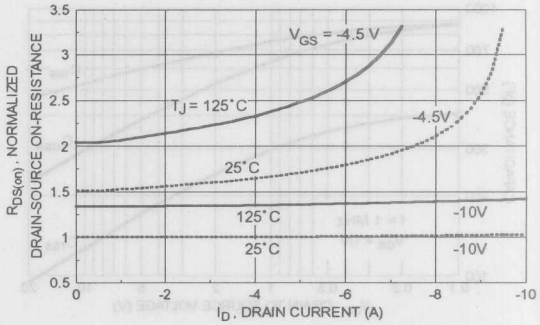


Figure 4. On-Resistance Variation with Drain Current and Temperature.

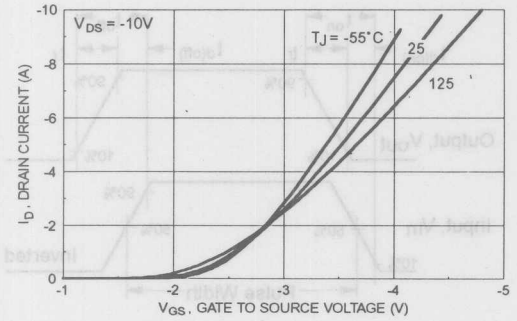


Figure 5. Drain Current Variation with Gate Voltage and Temperature.

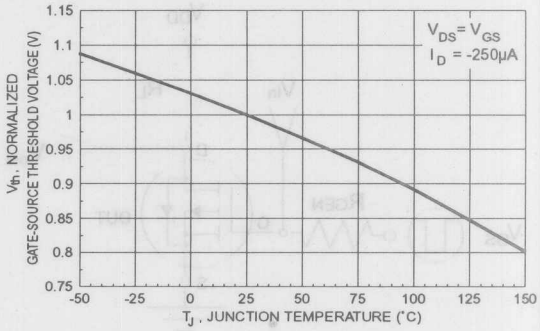


Figure 6. Gate Threshold Variation with Temperature.

Typical Electrical Characteristics (continued)

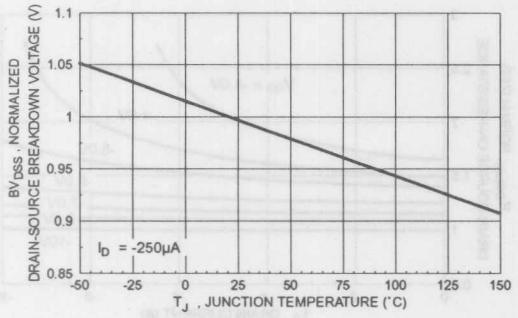


Figure 7. Breakdown Voltage Variation with Temperature.

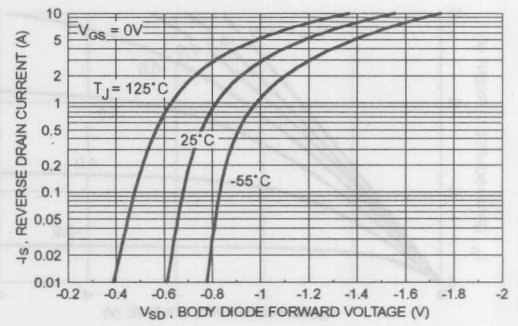


Figure 8. Body Diode Forward Voltage Variation with Current and Temperature

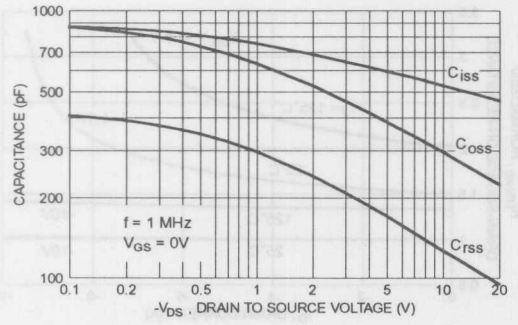


Figure 9. Capacitance Characteristics.

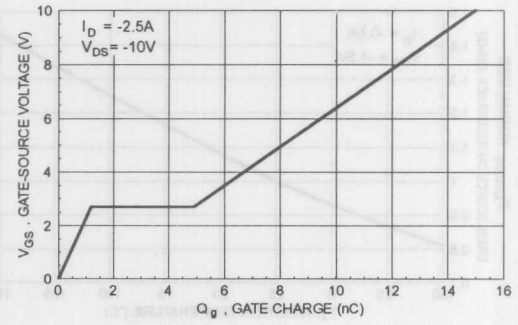


Figure 10. Gate Charge Characteristics.

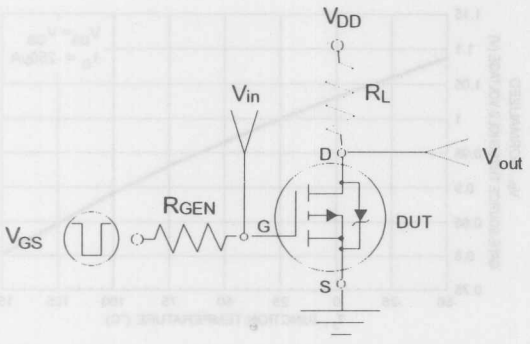


Figure 11. Switching Test Circuit

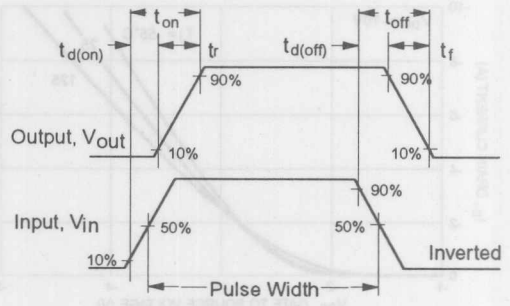


Figure 12. Switching Waveforms

Typical Electrical Characteristics (continued)

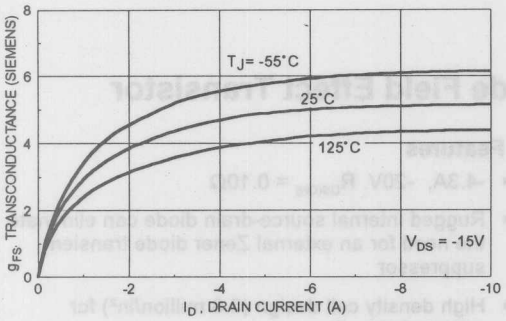


Figure 13. Transconductance Variation with Drain Current and Temperature.

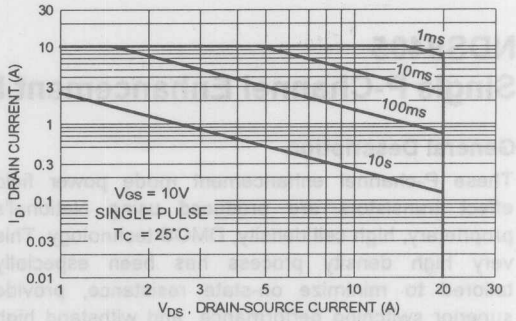


Figure 14. Maximum Safe Operating Area.

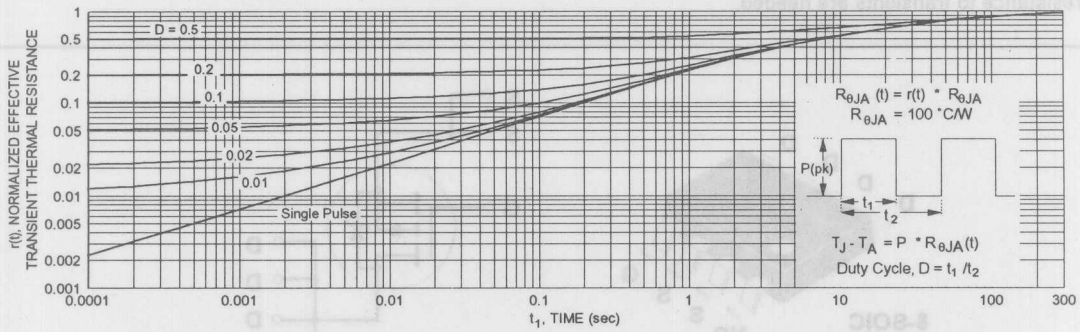


Figure 15. Transient Thermal Response Curve.

National Semiconductor

November 1993
PRELIMINARY

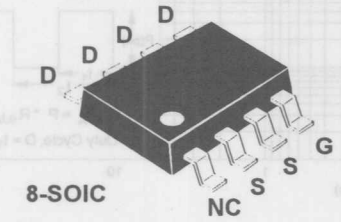
NDS9405
Single P-Channel Enhancement Mode Field Effect Transistor

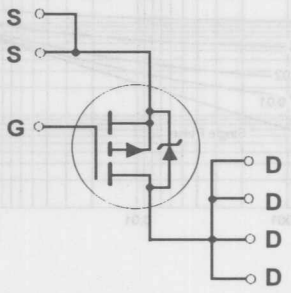
General Description

These P-channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulses in the avalanche and commutation modes. These devices are particularly suited for low voltage applications such as laptop computer power management and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- -4.3A, -20V. $R_{DS(ON)}$ = 0.10Ω
- Rugged internal source-drain diode can eliminate the need for an external Zener diode transient suppressor
- High density cell design (3.8 million/in²) for extremely low $R_{DS(ON)}$
- High power and current handling capability in a widely used surface mount package
- Critical DC electrical parameters specified at elevated temperature





ABSOLUTE MAXIMUM RATINGS T_C = 25°C unless otherwise noted

Symbol	Parameter	NDS9405	Units
V_{DSS}	Drain-Source Voltage	-20	V
V_{DGR}	Drain-Gate Voltage ($R_{GS} \leq 1$ MΩ)	-20	V
V_{GSS}	Gate-Source Voltage	± 20	V
I_D	Drain Current - Continuous @ T_A = 25°C	±4.3	A
	- Continuous @ T_A = 70°C	± 3.3	A
	- Pulsed	± 20	A
P_D	Maximum Power Dissipation @ T_A = 25°C	2.5 (Note 1)	W
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to 150	°C
THERMAL CHARACTERISTICS			
$R_{\theta JA}(t)$	Thermal Resistance, Junction-to-Ambient (Pulse = 10 seconds)	50 (Note 1)	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Steady-State)	100 (Note 2)	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = -250 µA	-20			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -16 V, V_{GS} = 0 V			-2	µA
		T_C = 55°C			-25	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note 3)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = -250 µA	-0.5	-2	-3	V
		T_C=125°C	-0.85	-1.7	-2.6	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = -10 V, I_D = -2 A		0.053	0.1	Ω
		T_C=125°C		0.075	0.15	Ω
		V_{GS} = -4.5 V, I_D = -2 A		0.08	0.16	Ω
		T_C=125°C		0.12	0.24	Ω
$I_{D(on)}$	On-State Drain Current	V_{GS} = -10 V, V_{DS} = -5 V	-20			A
		V_{GS} = -4.5, V_{DS} = -5V	-5			A
g_{FS}	Forward Transconductance	V_{DS} = -15 V, I_D = -4.3 A		8		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = -10 V, V_{GS} = 0 V, f = 1.0 MHz		1325		pF
C_{oss}	Output Capacitance			750		pF
C_{rss}	Reverse Transfer Capacitance			325		pF
SWITCHING CHARACTERISTICS (Note 3)						
$t_{D(ON)}$	Turn - On Delay Time	V_{DD} = -10 V, I_D = -1 A, V_{GEN} = -10 V, R_{GEN} = 6 Ω			30	ns
t_r	Turn - On Rise Time				80	ns
$t_{D(OFF)}$	Turn - Off Delay Time				200	ns
t_f	Turn - Off Fall Time				200	ns
Q_g	Total Gate Charge	V_{DS} = -10 V, I_D = -4.3A, V_{GS} = -10 V		38	40	nC
Q_{gs}	Gate-Source Charge			3	5	nC
Q_{gd}	Gate-Drain Charge			12	25	nC
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain-Source Diode Forward Current				-2.2	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = -1.25 A (Note 3)		-0.78	-1.6	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0V, I_S = -1.25 A, dI_S/dt = 100 A/µs		80		ns

Notes:

1. Maximum power dissipation and thermal resistance based on an assumption that a 10 second pulse is equivalent to steady-state and using a single-sided maximum-copper mounting board.
2. Junction-to-ambient thermal resistance based on steady-state conditions in still air using mounting board with minimum heat dissipation characteristics.
3. Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%.

National Semiconductor

July 1993
ADVANCE INFORMATION

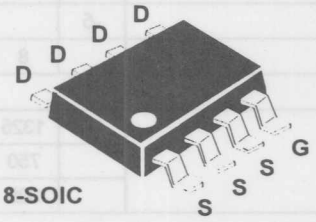
NDS9407
Single P-Channel Enhancement Mode Field Effect Transistor

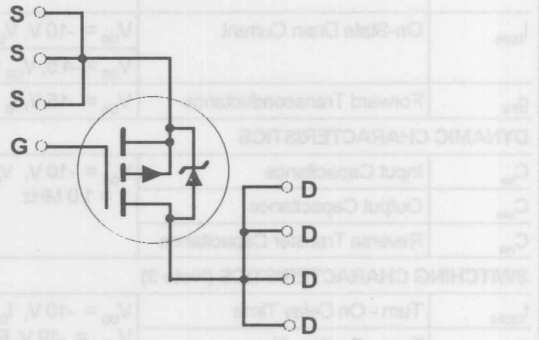
General Description

These P-channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulses in the avalanche and commutation modes. These devices are particularly suited for low voltage applications such as laptop computer power management and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- -3.3A, -60V. $R_{DS(ON)}$ = 0.15Ω.
- Rugged internal source-drain diode can eliminate the need for an external Zener diode transient suppressor.
- High density cell design (3.8 million/in²) for extremely low $R_{DS(ON)}$.
- High power and current handling capability in a widely used surface mount package.
- Critical DC electrical parameters specified at elevated temperature.





Absolute Maximum Ratings

T_C = 25°C unless otherwise noted

Symbol	Parameter	NDS9407	Units
V_{DSS}	Drain-Source Voltage	-60	V
V_{DGR}	Drain-Gate Voltage ($R_{GS} \leq 1$ MΩ)	-60	V
V_{GSS}	Gate-Source Voltage	± 20	V
I_D	Drain Current - Continuous @ T_A = 25°C	±3.3	A
	- Continuous @ T_A = 70°C	± 2.6	A
	- Pulsed	± 13	A
P_D	Maximum Power Dissipation @ T_A = 25°C	2.5 (Note 1)	W
T_J,T_{STG}	Operating and Storage Temperature Range	-55 to 150	°C
THERMAL CHARACTERISTICS			
$R_{\theta JA}(t)$	Thermal Resistance, Junction-to-Ambient (Surface Mounted. Pulse time = 10 seconds)	50 (Note 1)	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Surface Mounted. Steady-State)	TBD	°C/W

Electrical Characteristics (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = -250 µA	-60			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -48 V, V_{GS} = 0 V			-1	µA
		T_C = 55°C			-10	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = -250 µA	-1		-3	V
		T_C=125°C	TBD		TBD	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = -10 V, I_D = -3.3 A			0.15	Ω
		T_C=125°C			TBD	Ω
		V_{GS} = -4.5 V, I_D = -2.6 A			0.24	Ω
		T_C=125°C			TBD	Ω
$I_{D(on)}$	On-State Drain Current	V_{GS} = -10 V, V_{DS} = -10 V	-20			A
g_{FS}	Forward Transconductance	V_{DS} = -15 V, I_D = -3.3 A	5	TBD		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = -25 V, V_{GS} = 0 V, f = 1.0 MHz		TBD		pF
C_{oss}	Output Capacitance			TBD		pF
C_{rss}	Reverse Transfer Capacitance			TBD		pF
SWITCHING CHARACTERISTICS (Note 2)						
$t_{D(ON)}$	Turn - On Delay Time	V_{DD} = -25 V, I_D = -1 A, V_{GEN} = -10 V, R_{GEN} = 6 Ω			TBD	ns
t_r	Turn - On Rise Time				TBD	ns
$t_{D(OFF)}$	Turn - Off Delay Time				TBD	ns
t_f	Turn - Off Fall Time				TBD	ns
Q_g	Total Gate Charge	V_{DS} = -30 V, I_D = -3.3A, V_{GS} = -10 V		TBD		nC
Q_{gs}	Gate-Source Charge			TBD		nC
Q_{gd}	Gate-Drain Charge			TBD		nC
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain-Source Diode Forward Current				-2.2	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = -3.3A (Note 2)			-1.2	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0V, I_S = -3.3 A, dI_S/dt = 100 A/µs		TBD		ns
I_{rr}	Reverse Recovery Current			TBD		A

Notes:

1. Power dissipation and thermal resistance determinations based on an assumption that a 10 second pulse is equivalent to steady-state.
2. Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%.

National Semiconductor

November 1993

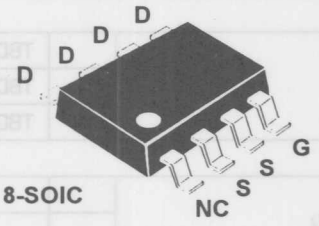
NDS9410
Single N-Channel Enhancement Mode Field Effect Transistor

General Description

These N-channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulses in the avalanche and commutation modes. These devices are particularly suited for low voltage applications such as laptop computer power management and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- 7.0A, 30V. $R_{DS(ON)}$ = 0.03Ω
- Rugged internal source-drain diode can eliminate the need for an external Zener diode transient suppressor
- High density cell design (3.8 million/in²) for extremely low $R_{DS(ON)}$
- High power and current handling capability in a widely used surface mount package
- Critical DC electrical parameters specified at elevated temperature



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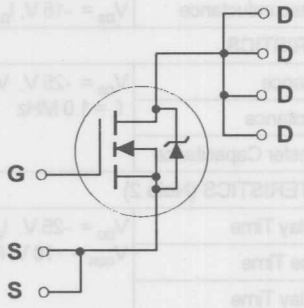


ABSOLUTE MAXIMUM RATINGS T_C = 25°C unless otherwise noted

Symbol	Parameter	NDS9410	Units
V_{DSS}	Drain-Source Voltage	30	V
V_{DGR}	Drain-Gate Voltage ($R_{GS} \leq 1$ MΩ)	30	V
V_{GSS}	Gate-Source Voltage	± 20	V
I_D	Drain Current - Continuous @ T_A = 25°C	±7.0	A
	- Continuous @ T_A = 70°C	± 5.8	A
	- Pulsed	± 20	A
P_D	Maximum Power Dissipation @ T_A = 25°C	2.5 (Note 1)	W
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to 150	°C
THERMAL CHARACTERISTICS			
$R_{\theta JA}(t)$	Thermal Resistance, Junction-to-Ambient (Pulse = 10 seconds)	50 (Note 1)	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Steady-State)	100 (Note 2)	°C/W

ELECTRICAL CHARACTERISTICS (T_c = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V			2	µA
		V_{DS} = 24 V, V_{GS} = 0 V, T_c = 55°C			25	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note 3)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	1	1.4	3	V
		V_{DS} = V_{GS}, I_D = 250 µA, T_c=125°C	0.7	1	2.2	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 7.0 A		0.022	0.03	Ω
		V_{GS} = 10 V, I_D = 7.0 A, T_c=125°C		0.033	0.045	Ω
		V_{GS} = 4.5 V, I_D = 3.5 A		0.031	0.05	Ω
		V_{GS} = 4.5 V, I_D = 3.5 A, T_c=125°C		0.045	0.075	Ω
$I_{D(on)}$	On-State Drain Current	V_{GS} = 10 V, V_{DS} = 5 V	20			A
		V_{GS} = 2.7, V_{DS} = 2.7V		7.7		A
g_{FS}	Forward Transconductance	V_{DS} = 15 V, I_D = 7.0 A		15		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 15 V, V_{GS} = 0 V, f = 1.0 MHz		1250		pF
C_{oss}	Output Capacitance			610		pF
C_{rss}	Reverse Transfer Capacitance			260		pF
SWITCHING CHARACTERISTICS (Note 3)						
$t_{D(ON)}$	Turn - On Delay Time	V_{DD} = 25 V, I_D = 1 A, V_{GEN} = 10 V, R_{GEN} = 6 Ω		10	30	ns
t_r	Turn - On Rise Time			15	60	ns
$t_{D(OFF)}$	Turn - Off Delay Time			70	150	ns
t_f	Turn - Off Fall Time			50	140	ns
Q_g	Total Gate Charge	V_{DS} = 15 V, I_D = 2.0A, V_{GS} = 10 V		41	50	nC
Q_{gs}	Gate-Source Charge			2.8		nC
Q_{gd}	Gate-Drain Charge			12		nC
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain-Source Diode Forward Current				2.2	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 2.0 A (Note 3)		0.76	1.1	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0V, I_S = 2 A, dI_S/dt = 100 A/µs		100		ns

Notes:

1. Maximum power dissipation and thermal resistance based on an assumption that a 10 second pulse is equivalent to steady-state and using a single-sided maximum-copper mounting board.
2. Junction-to-ambient thermal resistance based on steady-state conditions in still air using mounting board with minimum heat dissipation characteristics.
3. Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%.

TYPICAL ELECTRICAL CHARACTERISTICS

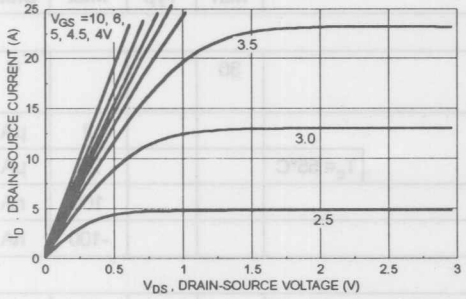


Figure 1. On-Region Characteristics

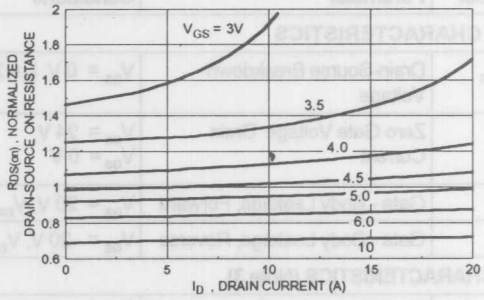


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

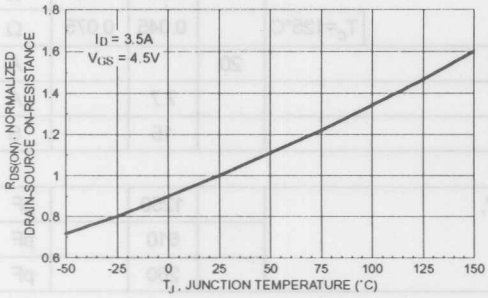


Figure 3. On-Resistance Variation with Temperature

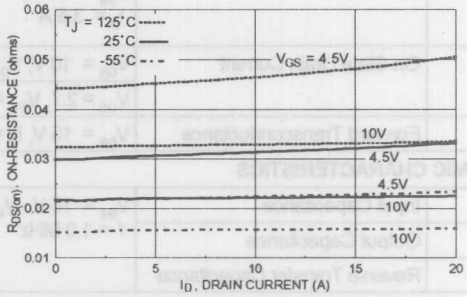


Figure 4. On-Resistance Variation with Drain Current and Temperature

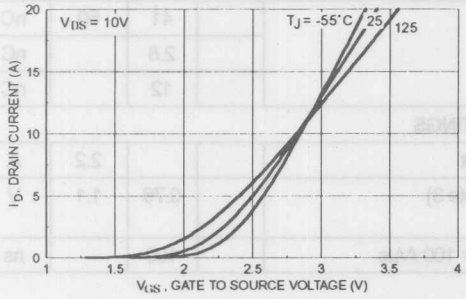


Figure 5. Transfer Charateristics

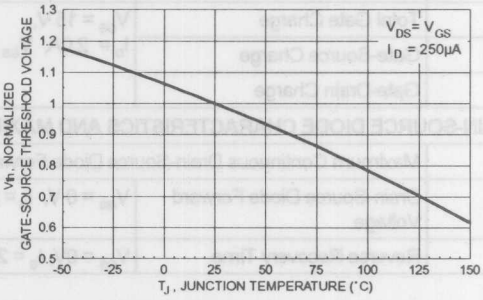


Figure 6. Gate Threshold Variation with Temperature

TYPICAL ELECTRICAL CHARACTERISTICS (continued)

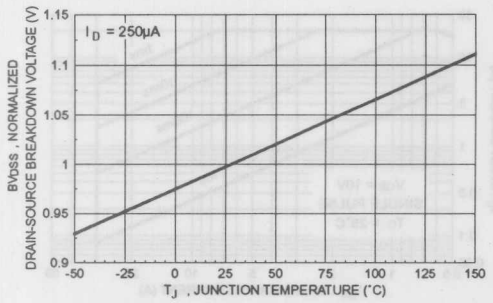


Figure 7. Breakdown Voltage Variation with Temperature

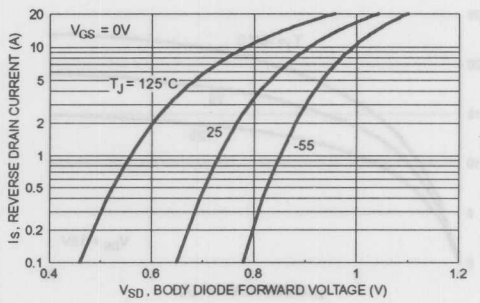


Figure 8. Body Diode Forward Voltage Variation with Source Current and Temperature

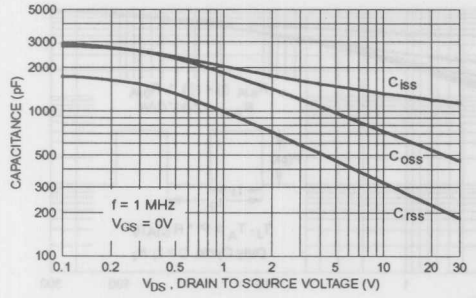


Figure 9. Capacitance Characteristics

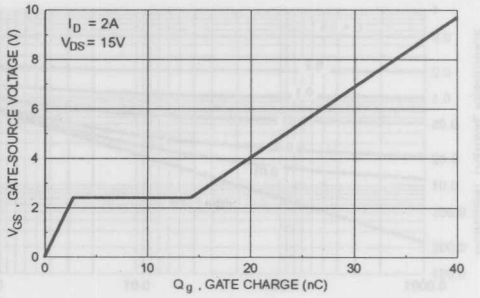


Figure 10. Gate Charge Characteristics

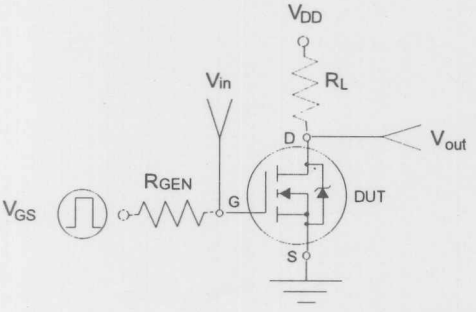


Figure 11. Switching Test Circuit

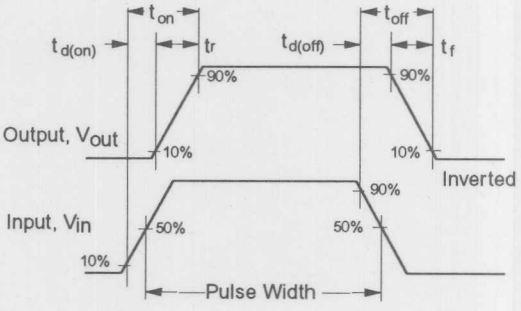


Figure 12. Switching Waveforms

TYPICAL ELECTRICAL CHARACTERISTICS (continued)

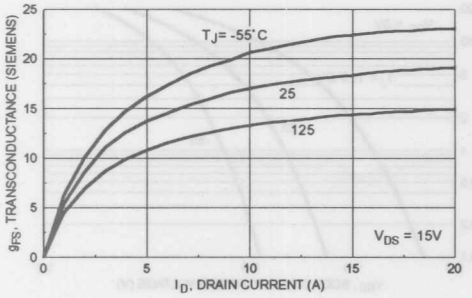


Figure 13. Transconductance Variation with Drain Current and Temperature

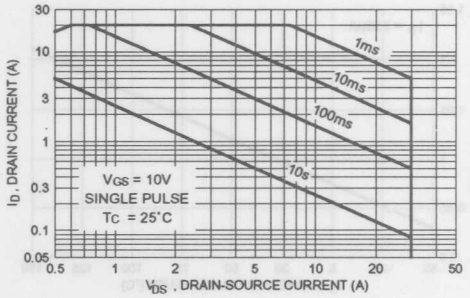


Figure 14. Maximum Safe Operating Area

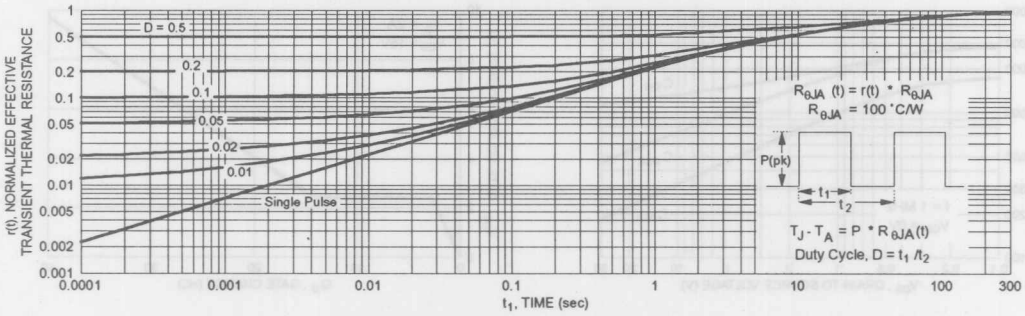


Figure 15. Thermal Response

National Semiconductor

November 1993
PRELIMINARY

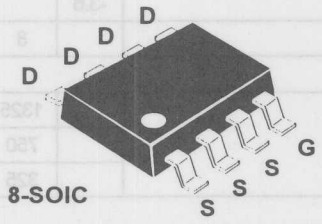
NDS9430
Single P-Channel Enhancement Mode Field Effect Transistor

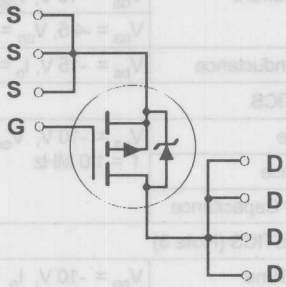
General Description

These P-channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulses in the avalanche and commutation modes. These devices are particularly suited for low voltage applications such as laptop computer power management and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- -5.3A, -20V. $R_{DS(ON)}$ = 0.06Ω
- Rugged internal source-drain diode can eliminate the need for an external Zener diode transient suppressor
- High density cell design (3.8 million/in²) for extremely low $R_{DS(ON)}$
- High power and current handling capability in a widely used surface mount package
- Critical DC electrical parameters specified at elevated temperature





ABSOLUTE MAXIMUM RATINGS T_C = 25°C unless otherwise noted

Symbol	Parameter	NDS9430	Units
V_{DSS}	Drain-Source Voltage	-20	V
V_{DGR}	Drain-Gate Voltage ($R_{GS} \leq 1$ MΩ)	-20	V
V_{GSS}	Gate-Source Voltage	± 20	V
I_D	Drain Current - Continuous @ T_A = 25°C	±5.3	A
	- Continuous @ T_A = 70°C	± 4.2	A
	- Pulsed	± 15	A
P_D	Maximum Power Dissipation @ T_A = 25°C	2.5 (Note 1)	W
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to 150	°C
THERMAL CHARACTERISTICS			
$R_{\theta JA}(t)$	Thermal Resistance, Junction-to-Ambient (Pulse = 10 seconds)	50 (Note 1)	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Steady-State)	100 (Note 2)	°C/W

ELECTRICAL CHARACTERISTICS (T_c = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = -250 µA	-20			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -16 V, V_{GS} = 0 V			-1	µA
		T_c = 55°C			-10	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note 3)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = -250 µA	-1	-2	-3	V
		T_c=125°C	-0.85	-1.7	-2.6	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = -10 V, I_D = -5.3 A		0.055	0.06	Ω
		T_c=125°C		0.077	0.09	Ω
		V_{GS} = -6 V, I_D = -3.6 A		0.067	0.08	Ω
		V_{GS} = -4.5 V, I_D = -2 A		0.082	0.125	Ω
		T_c=125°C		0.12	0.19	Ω
$I_{D(on)}$	On-State Drain Current	V_{GS} = -10 V, V_{DS} = -5 V	-15			A
		V_{GS} = -4.5, V_{DS} = -5V	-3.6			A
g_{FS}	Forward Transconductance	V_{DS} = -15 V, I_D = -5.3 A		8		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = -10 V, V_{GS} = 0 V, f = 1.0 MHz		1325		pF
C_{oss}	Output Capacitance			750		pF
C_{rss}	Reverse Transfer Capacitance			325		pF
SWITCHING CHARACTERISTICS (Note 3)						
$t_{D(ON)}$	Turn - On Delay Time	V_{DD} = -10 V, I_D = -1 A, V_{GEN} = -10 V, R_{GEN} = 6 Ω			30	ns
t_r	Turn - On Rise Time				60	ns
$t_{D(OFF)}$	Turn - Off Delay Time				120	ns
t_f	Turn - Off Fall Time				100	ns
Q_g	Total Gate Charge	V_{DS} = -10 V, I_D = -5.3A, V_{GS} = -10 V		38		nC
Q_{gs}	Gate-Source Charge			3		nC
Q_{gd}	Gate-Drain Charge			12		nC
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain-Source Diode Forward Current				-2.2	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_s = -5.3 A (Note 3)		-1.04	-1.2	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0V, I_S = -5.3 A, dI_S/dt = 100 A/µs		80	100	ns

Notes:

1. Maximum power dissipation and thermal resistance based on an assumption that a 10 second pulse is equivalent to steady-state and using a single-sided maximum-copper mounting board.
2. Junction-to-ambient thermal resistance based on steady-state conditions in still air using mounting board with minimum heat dissipation characteristics.
3. Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%.

National Semiconductor

November 1993
PRELIMINARY

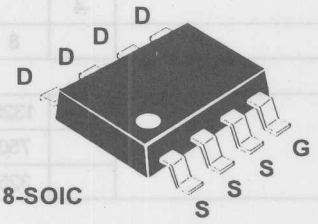
NDS9435
Single P-Channel Enhancement Mode Field Effect Transistor

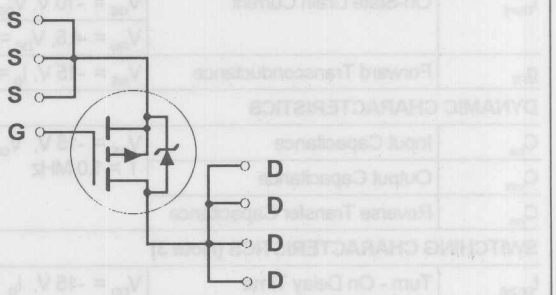
General Description

These P-channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulses in the avalanche and commutation modes. These devices are particularly suited for low voltage applications such as laptop computer power management and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- -4.6A, -30V. $R_{DS(ON)}$ = 0.07Ω
- Rugged internal source-drain diode can eliminate the need for an external Zener diode transient suppressor
- High density cell design (3.8 million/in²) for extremely low $R_{DS(ON)}$
- High power and current handling capability in a widely used surface mount package
- Critical DC electrical parameters specified at elevated temperature





ABSOLUTE MAXIMUM RATINGS T_c = 25°C unless otherwise noted

Symbol	Parameter	NDS9435	Units
V_{DSS}	Drain-Source Voltage	-30	V
V_{DGR}	Drain-Gate Voltage ($R_{GS} \leq 1$ MΩ)	-30	V
V_{GSS}	Gate-Source Voltage	± 20	V
I_D	Drain Current - Continuous @ T_A = 25°C	±4.6	A
	- Continuous @ T_A = 70°C	± 4.1	A
	- Pulsed	± 15	A
P_D	Maximum Power Dissipation @ T_A = 25°C	2.5 (Note 1)	W
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to 150	°C
THERMAL CHARACTERISTICS			
$R_{\theta JA}(t)$	Thermal Resistance, Junction-to-Ambient (Pulse = 10 seconds)	50 (Note 1)	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Steady-State)	100 (Note 2)	°C/W

ELECTRICAL CHARACTERISTICS (T_c = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = -250 µA	-30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -24 V, V_{GS} = 0 V			-1	µA
		T_c = 55°C			-10	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note 3)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = -250 µA	-1	-2	-3	V
		T_c=125°C	-0.85	-1.7	-2.6	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = -10 V, I_D = -4.6 A		0.054	0.07	Ω
		T_c=125°C		0.075	0.105	Ω
		V_{GS} = -6 V, I_D = -4.1 A		0.068	0.09	Ω
		V_{GS} = -4.5 V, I_D = -2 A		0.083	0.135	Ω
		T_c=125°C		0.12	0.2	Ω
$I_{D(on)}$	On-State Drain Current	V_{GS} = -10 V, V_{DS} = -5 V	-15			A
		V_{GS} = -4.5, V_{DS} = -5V	-4			A
g_{FS}	Forward Transconductance	V_{DS} = -15 V, I_D = -4.6 A		8		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = -15 V, V_{GS} = 0 V, f = 1.0 MHz		1325		pF
C_{oss}	Output Capacitance			750		pF
C_{rss}	Reverse Transfer Capacitance			325		pF
SWITCHING CHARACTERISTICS (Note 3)						
$t_{D(ON)}$	Turn - On Delay Time	V_{DD} = -15 V, I_D = -1 A, V_{GEN} = -10 V, R_{GEN} = 6 Ω			30	ns
t_r	Turn - On Rise Time				60	ns
$t_{D(OFF)}$	Turn - Off Delay Time				120	ns
t_f	Turn - Off Fall Time				100	ns
Q_g	Total Gate Charge	V_{DS} = -10 V, I_D = -4.6A, V_{GS} = -10 V		38	40	nC
Q_{gs}	Gate-Source Charge			3		nC
Q_{gd}	Gate-Drain Charge			12		nC
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain-Source Diode Forward Current				-2.2	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = -4.6 A (Note 3)		-1	-1.2	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0V, I_S = -4.6 A, dI_S/dt = 100 A/µs		80	100	ns

Notes:

1. Maximum power dissipation and thermal resistance based on an assumption that a 10 second pulse is equivalent to steady-state and using a single-sided maximum-copper mounting board.
2. Junction-to-ambient thermal resistance based on steady-state conditions in still air using mounting board with minimum heat dissipation characteristics.
3. Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%.

National Semiconductor

January 1994

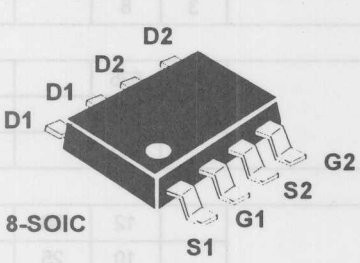
NDS9936
Dual P-Channel Enhancement Mode Field Effect Transistor

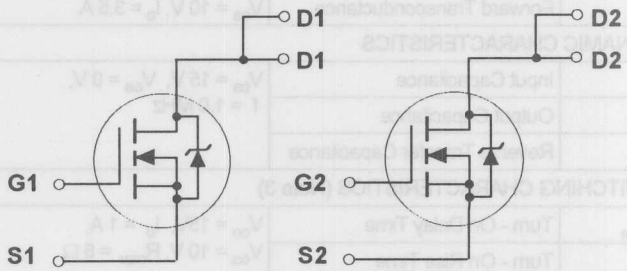
General Description

These n-channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulses in the avalanche and commutation modes. These devices are particularly suited for low voltage applications such as laptop computer power management and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- 5A, 30V. $R_{DS(ON)}$ = 0.05Ω.
- Rugged internal source-drain diode can eliminate the need for an external Zener diode transient suppressor.
- High density cell design (3.8 million/in²) for extremely low $R_{DS(ON)}$.
- High power and current handling capability in a widely used surface mount package.
- Dual MOSFET in surface mount package
- Critical DC electrical parameters specified at elevated temperature





Absolute Maximum Ratings

T_C = 25°C unless otherwise noted

Symbol	Parameter	NDS9936	Units
V_{DSS}	Drain-Source Voltage	30	V
V_{DGR}	Drain-Gate Voltage ($R_{GS} \leq 1$ MΩ)	30	V
V_{GSS}	Gate-Source Voltage	± 20	V
I_D	Drain Current - Continuous @ T_A = 25°C	± 5.0	A
	- Continuous @ T_A = 70°C	± 4.0	A
	- Pulsed	± 40	A
P_D	Total Power Dissipation @ T_C = 25°C	2 (Note 1)	W
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to 150	°C
THERMAL CHARACTERISTICS			
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Pulse time = 10 seconds)	62.5 (Note 1)	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Steady-State)	100 (Note 2)	°C/W

Electrical Characteristics (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V			2	µA
		V_{DS} = 24 V, V_{GS} = 0 V, T_C = 55°C			20	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note 3)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	1		3	V
		V_{DS} = V_{GS}, I_D = 250 µA, T_C=125°C	0.7		2.2	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 5 A			0.05	Ω
		V_{GS} = 10 V, I_D = 5 A, T_C=125°C			0.1	Ω
		V_{GS} = 4.5 V, I_D = 3.9 A			0.08	Ω
		V_{GS} = 4.5 V, I_D = 3.9 A, T_C=125°C			0.16	Ω
$I_{D(on)}$	On-State Drain Current	V_{GS} = 10 V, V_{DS} = 10 V	40			A
		V_{GS} = 4.5 V, V_{DS} = 10 V	20			A
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 3.5 A	3	8		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 15 V, V_{GS} = 0 V, f = 1.0 MHz		525		pF
C_{oss}	Output Capacitance			315		pF
C_{rss}	Reverse Transfer Capacitance			185		pF
SWITCHING CHARACTERISTICS (Note 3)						
$t_{D(ON)}$	Turn - On Delay Time	V_{DD} = 15V, I_D = 1 A, V_{GS} = 10 V, R_{GEN} = 6 Ω		12	30	ns
t_r	Turn - On Rise Time			10	25	ns
$t_{D(OFF)}$	Turn - Off Delay Time			25	50	ns
t_f	Turn - Off Fall Time			10	50	ns
Q_g	Total Gate Charge	V_{DS} = 15 V, I_D = 5 A, V_{GS} = 10 V		17	35	nC
Q_{gs}	Gate-Source Charge			1.5		nC
Q_{gd}	Gate-Drain Charge			3.7		nC
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuos Drain-Source Diode Forward Current				1.7	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 1.7 A (Note 3)		0.78	1.2	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0V, I_S = 5 A, dI_S/dt = 100 A/µs		70	160	ns

Notes:

1. Power dissipation and thermal resistance determinations based on an assumption that a 10 second pulse is equivalent to steady-state and using a single-sided maximum copper mounting board.
2. Junnction-to-ambient thermal resistance based on steady-state conditions in still air using mounting board with minimum heat dissipation characteristics.
3. Pulse Test: Pulse Width ≤ 300 ms, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

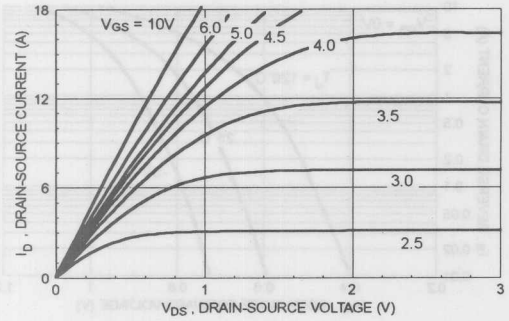


Figure 1. On-Region Characteristics.

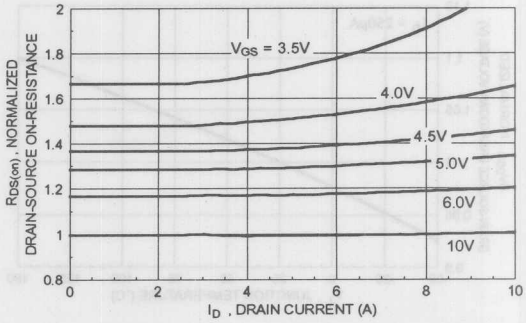


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current.

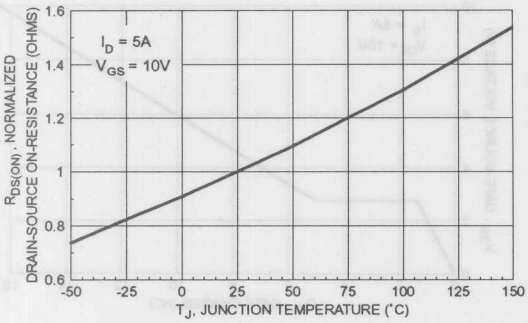


Figure 3. On-Resistance Variation with Temperature.

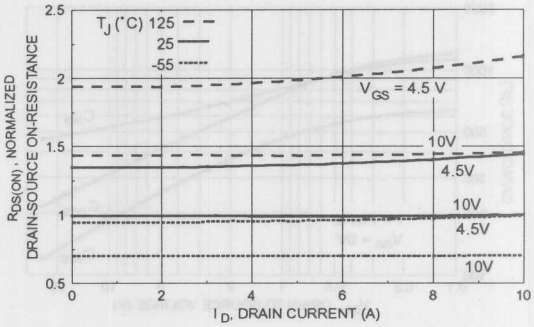


Figure 4. On-Resistance Variation with Drain Current and Temperature.

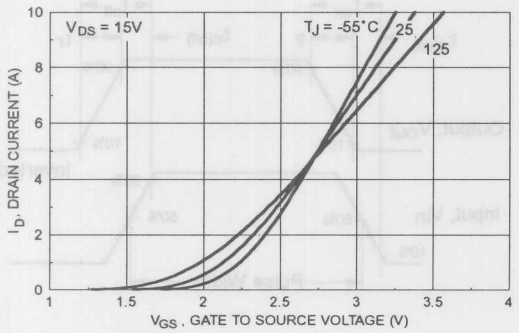


Figure 5. Transfer Characteristics.

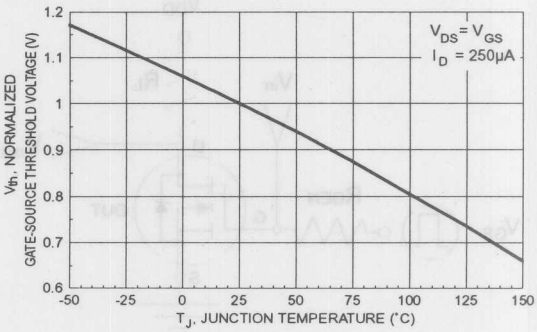


Figure 6. Gate Threshold Variation with Temperature.

Typical Electrical Characteristics (continued)

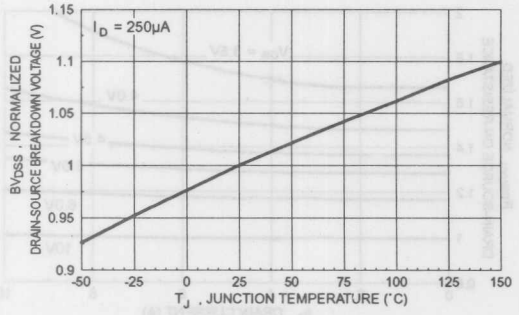


Figure 7. Breakdown Voltage Variation with Temperature.

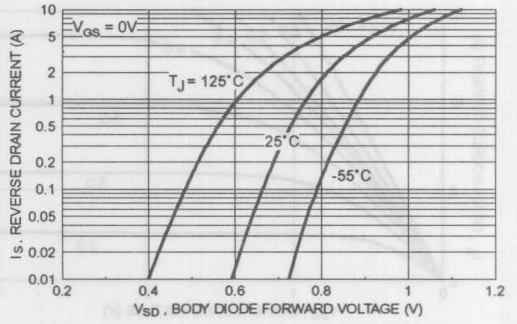


Figure 8. Body Diode Forward Voltage Variation with Current and Temperature

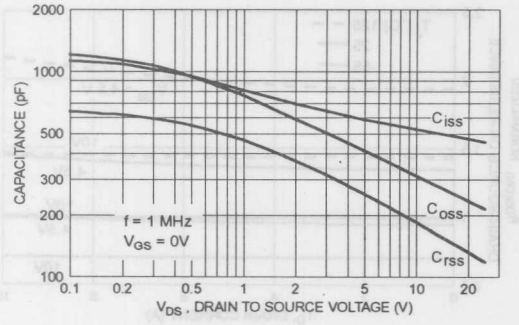


Figure 9. Capacitance Characteristics.

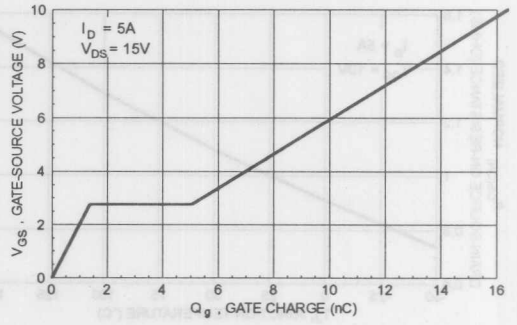


Figure 10. Gate Charge Characteristics.

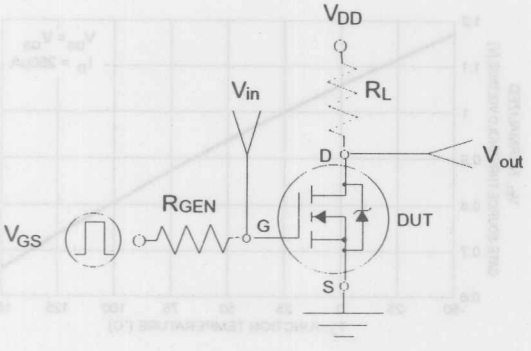


Figure 11. Switching Test Circuit

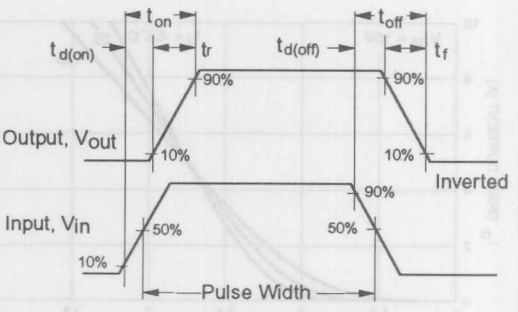


Figure 12. Switching Waveforms

Typical Electrical Characteristics (continued)

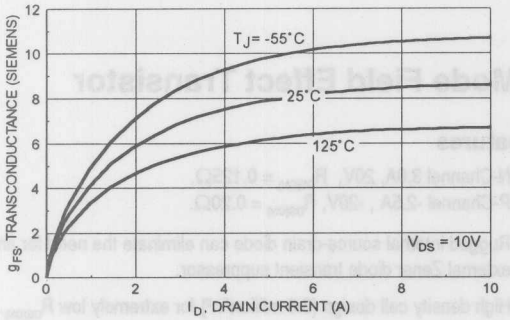


Figure 13. Transconductance Variation

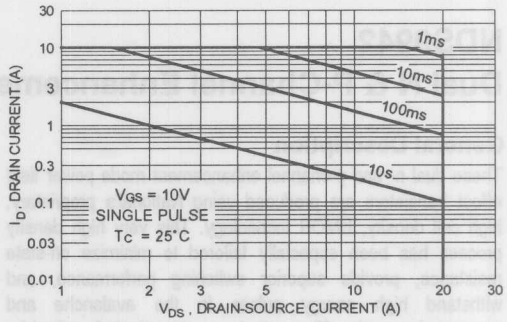


Figure 14. Maximum Safe Operating Area.

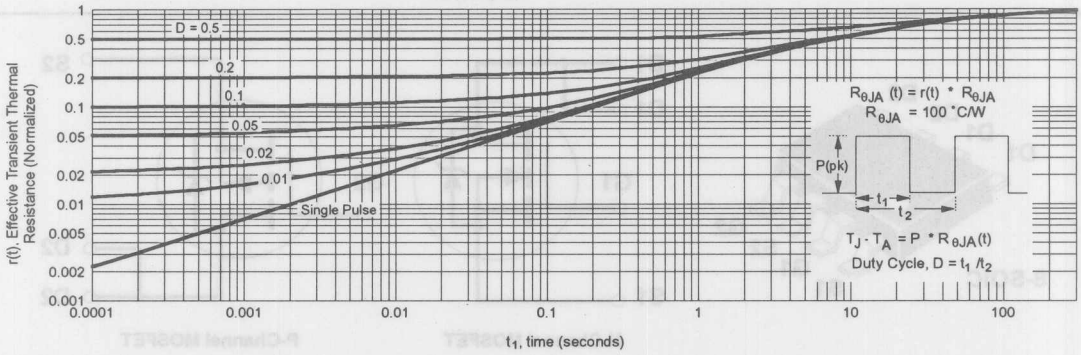


Figure 15. Transient Thermal Response Curve for Surface-Mounted Device.

National Semiconductor

August 1993

NDS9942

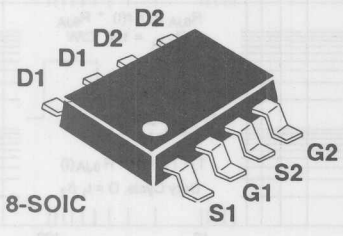
Dual N & P-Channel Enhancement Mode Field Effect Transistor

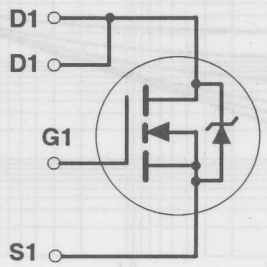
General Description

These dual n- and p-channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulses in the avalanche and commutation modes. These devices are particularly suited for low voltage applications such as laptop computer power management and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

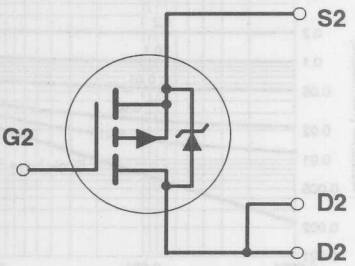
Features

- N-Channel 3.0A, 20V, $R_{DS(ON)}$ = 0.125Ω.
  P-Channel -2.5A , -20V, $R_{DS(ON)}$ = 0.20Ω.
- Rugged internal source-drain diode can eliminate the need for an external Zener diode transient suppressor.
- High density cell design (3.8 million/in²) for extremely low $R_{DS(ON)}$.
- High power and current handling capability in a widely used surface mount package.
- Dual (N & P-Channel) MOSFET in surface mount package.
- Critical DC electrical parameters specified at elevated temperature.





N-Channel MOSFET



P-Channel MOSFET

Absolute Maximum Ratings

T_C = 25°C unless otherwise noted

Symbol	Parameter	N-Channel	P-Channel	Units
V_{DSS}	Drain-Source Voltage	20	-20	V
V_{DGR}	Drain-Gate Voltage (R_{GS} ≤ 1 MΩ)	20	-20	V
V_{GSS}	Gate-Source Voltage	± 20	± 20	V
I_D	Drain Current - Continuous @ T_A = 25°C	± 3.0	± 2.5	A
	- Continuous @ T_A = 70°C	± 2.5	± 2.0	A
	- Pulsed	± 10	± 10	A
P_D	Maximum Power Dissipation @ T_A = 25°C	2 (Note 1)		W
T_J,T_{STG}	Operating and Storage Temperature Range	-55 to 150		°C
THERMAL CHARACTERISTICS				
$R_{\theta JA}$(t)	Thermal Resistance, Junction-to-Ambient (Surface Mounted. Pulse time = 10 seconds)	62.5 (Note 1)		°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Surface Mounted. Steady-State)	100		°C/W

Electrical Characteristics (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Type	Min	Typ	Max	Units
OFF CHARACTERISTICS							
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	N-Ch	20			V
		V_{GS} = 0 V, I_D = -250 µA	P-Ch	-20			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 16 V, V_{GS} = 0 V	N-Ch			2	µA
		V_{DS} = 16 V, V_{GS} = 0 V, T_C = 55°C	N-Ch			25	µA
		V_{DS} = -16 V, V_{GS} = 0 V	P-Ch			-2	µA
		V_{DS} = -16 V, V_{GS} = 0 V, T_C = 55°C	P-Ch			-25	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V	All			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS} = 0 V	All			-100	nA
ON CHARACTERISTICS (Note 2)							
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	N-Ch	1	1.5	3	V
		V_{DS} = V_{GS}, I_D = 250 µA, T_C=125°C	N-Ch	0.7	1.1	2.2	V
		V_{DS} = V_{GS}, I_D = -250 µA	P-Ch	-1	-2	-3	V
		V_{DS} = V_{GS}, I_D = -250 µA, T_C=125°C	P-Ch	-0.85	-1.7	-2.6	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 1.0 A	N-Ch		0.062	0.125	Ω
		V_{GS} = 10 V, I_D = 1.0 A, T_C=125°C	N-Ch		0.085	0.175	Ω
		V_{GS} = 4.5 V, I_D = 0.5 A	N-Ch		0.08	0.25	Ω
		V_{GS} = 4.5 V, I_D = 0.5 A, T_C=125°C	N-Ch		0.11	0.35	Ω
		V_{GS} = -10 V, I_D = -1.0 A	P-Ch		0.18	0.2	Ω
		V_{GS} = -10 V, I_D = -1.0 A, T_C=125°C	P-Ch		0.24	0.35	Ω
		V_{GS} = -4.5 V, I_D = -0.5 A	P-Ch		0.26	0.4	Ω
		V_{GS} = -4.5 V, I_D = -0.5 A, T_C=125°C	P-Ch		0.35	0.56	Ω
$I_{D(on)}$	On-State Drain Current	V_{GS} = 10 V, V_{DS} = 5 V	N-Ch	10			A
		V_{GS} = 4.5 V, V_{DS} = 5 V	N-Ch	2			A
		V_{GS} = -10 V, V_{DS} = -5 V	P-Ch	-10			A
		V_{GS} = -4.5V, V_{DS} = -5 V	P-Ch	-2			A
g_{FS}	Forward Transconductance	V_{DS} = 15 V, I_D = 3 A	N-Ch		7		S
		V_{DS} = -15 V, I_D = -3 A	P-Ch		4		S
DYNAMIC CHARACTERISTICS							
C_{iss}	Input Capacitance	N-Channel V_{DS} = 10V, V_{GS} = 0 V, f = 1.0 MHz	N-Ch		525		pF
		P-Channel V_{DS} = -10 V, V_{GS} = 0 V, f = 1.0 MHz	P-Ch		525		pF
C_{oss}	Output Capacitance	N-Channel V_{DS} = 10V, V_{GS} = 0 V, f = 1.0 MHz	N-Ch		315		pF
		P-Channel V_{DS} = -10 V, V_{GS} = 0 V, f = 1.0 MHz	P-Ch		300		pF
C_{rss}	Reverse Transfer Capacitance	N-Channel V_{DS} = 10V, V_{GS} = 0 V, f = 1.0 MHz	N-Ch		185		pF
		P-Channel V_{DS} = -10 V, V_{GS} = 0 V, f = 1.0 MHz	P-Ch		130		pF

Electrical Characteristics (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Type	Min	Typ	Max	Units
SWITCHING CHARACTERISTICS (Note 2)							
$t_{D(ON)}$	Turn - On Delay Time	N-Channel V_{DD} = 10 V, I_D = 1 A, V_{GEN} = 10 V, R_{GEN} = 6 Ω	N-Ch		6	15	ns
			P-Ch		8	40	ns
t_r	Turn - On Rise Time		N-Ch		12	20	ns
		P-Channel V_{DD} = -10 V, I_D = -1 A, V_{GEN} = -10 V, R_{GEN} = 6 Ω	P-Ch		15	40	ns
$t_{D(OFF)}$	Turn - Off Delay Time		N-Ch		22	50	ns
			P-Ch		25	90	ns
t_f	Turn - Off Fall Time		N-Ch		8	50	ns
			P-Ch		8	50	ns
Q_g	Total Gate Charge	N-Channel V_{DS} = 10V, I_D = 2.3A, V_{GS} = 10 V	N-Ch		17	27	nC
			P-Ch		15	25	nC
Q_{gs}	Gate-Source Charge		N-Ch		1.2		nC
		P-Channel V_{DS} = -10V, I_D = -2.3A, V_{GS} = -10 V	P-Ch		1.2		nC
Q_{gd}	Gate-Drain Charge		N-Ch		5		nC
			P-Ch		4.8		nC
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS							
I_S	Maximum Continuous Drain-Source Diode Forward Current		N-Ch			1.6	A
			P-Ch			-1.6	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 1.25 A (Note 2)	N-Ch		0.78	1.2	V
		V_{GS} = 0 V, I_S = -1.25 A (Note 2)	P-Ch		-0.94	-1.6	V
t_{rr}	Reverse Recovery Time	N-Channel V_{GS} = 0V, I_S = 1.25 A, dI_S/dt = 100 A/µs	N-Ch		28	100	ns
			P-Ch		29	100	ns
I_{rr}	Reverse Recovery Current	P-Channel V_{GS} = 0V, I_S = -1.25 A, dI_S/dt = 100 A/µs	N-Ch		2.1		A
			P-Ch		1.9		A

Notes:
1. Power dissipation and thermal resistance determinations based on an assumption that a 10 second pulse is equivalent to steady-state.
2. Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics: N-Channel

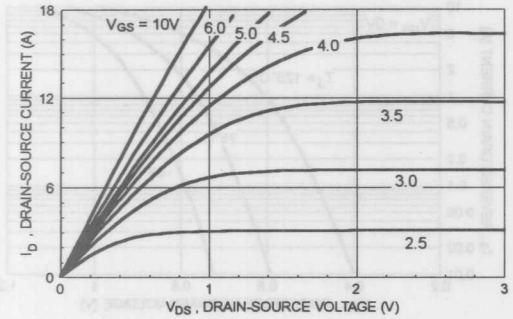


Figure 1. N-Channel On-Region Characteristic.

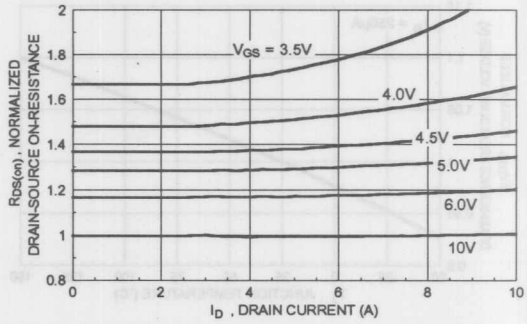


Figure 2. N-Channel On-Resistance Variation with Gate Voltage and Drain Current.

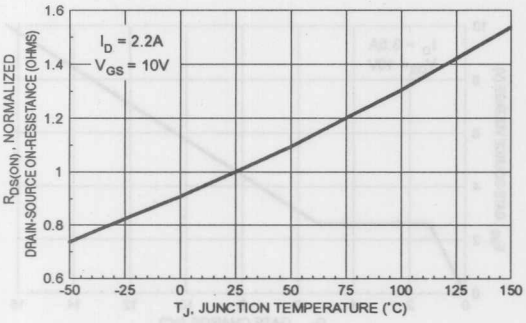


Figure 3. N-Channel On-Resistance Variation with Temperature.

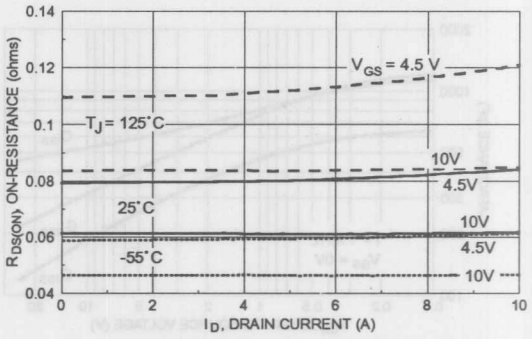


Figure 4. N-Channel On-Resistance Variation with Drain Current and Temperature.

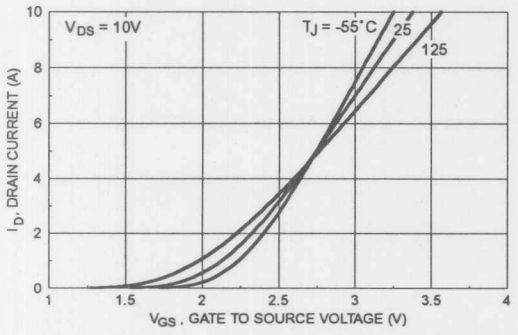


Figure 5. N-Channel Transfer Characteristic.

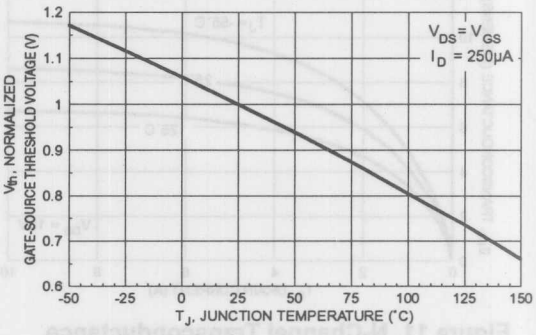


Figure 6. N-Channel Gate Threshold Variation with Temperature.

Typical Electrical Characteristics: N-Channel (continued)

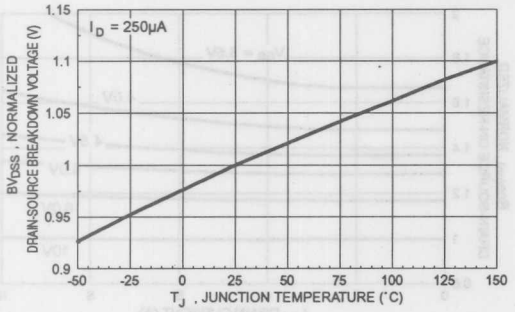


Figure 7. N-Channel Breakdown Voltage Variation with Temperature.

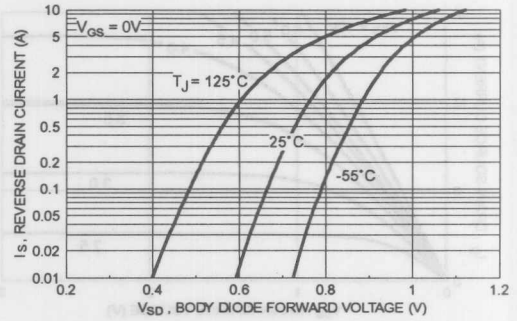


Figure 8. N-Channel Body Diode Forward Voltage Variation with Current and Temperature.

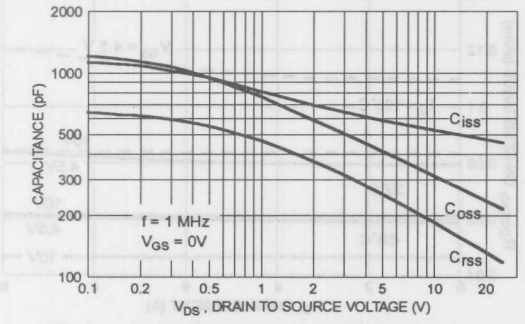


Figure 9. N-Channel Capacitance Characteristics.

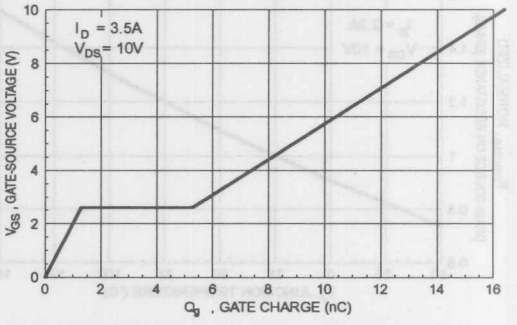


Figure 10. N-Channel Gate Charge Characteristic.

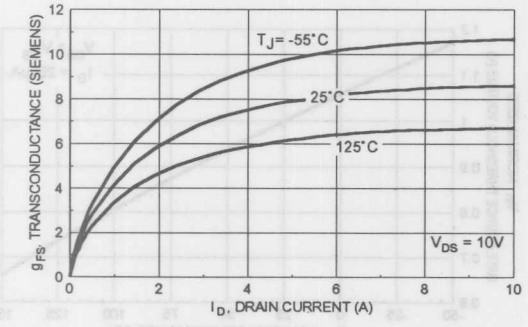


Figure 11. N-Channel Transconductance Variation with Drain Current and Temperature.

Typical Electrical Characteristics: P-Channel (continued)

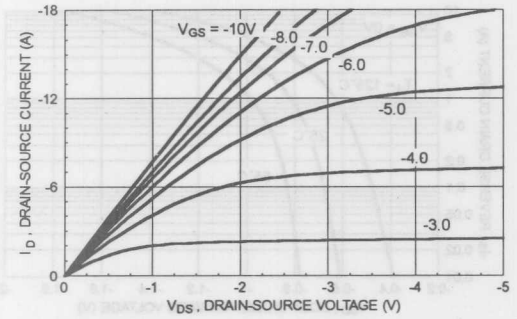


Figure 12. P-Channel On-Region Characteristics.

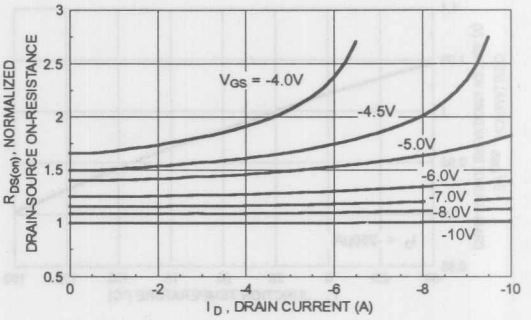


Figure 13. P-Channel On-Resistance Variation with Gate Voltage and Drain Current.

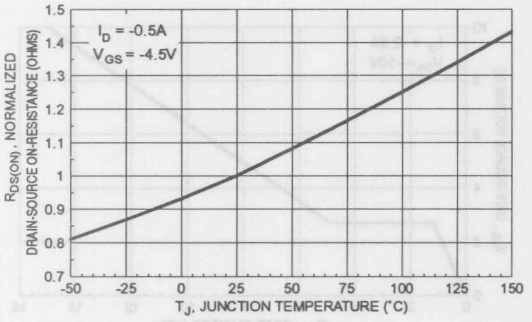


Figure 14. P-Channel On-Resistance Variation with Temperature.

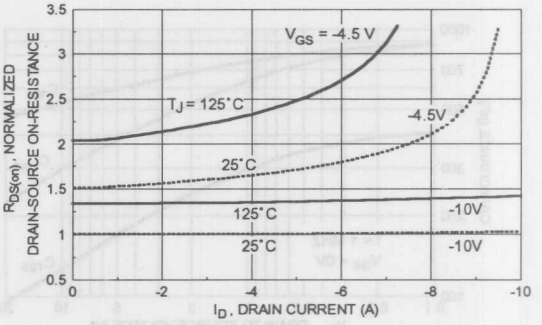


Figure 15. P-Channel On-Resistance Variation with Drain Current and Temperature.

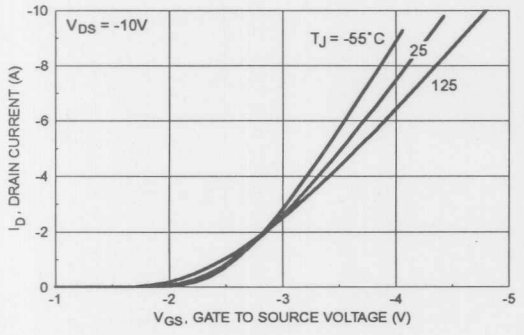


Figure 16. P-Channel Transfer Characteristics.

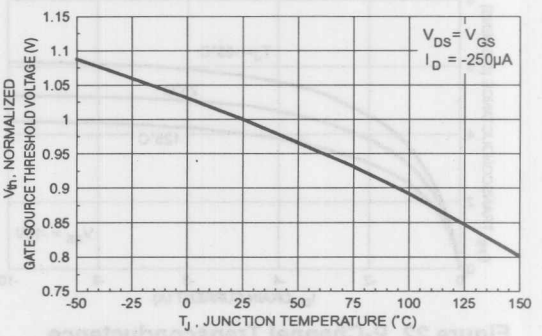


Figure 17. P-Channel Gate Threshold Variation with Temperature.

Typical Electrical Characteristics: P-Channel (continued)

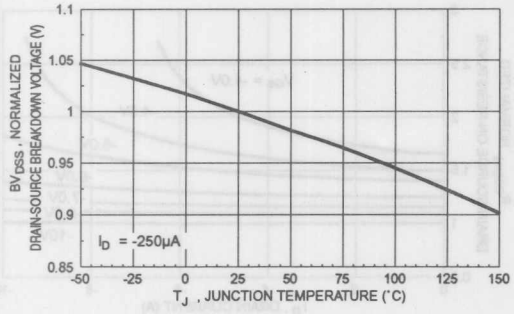


Figure 18. P-Channel Breakdown Voltage Variation with Temperature.

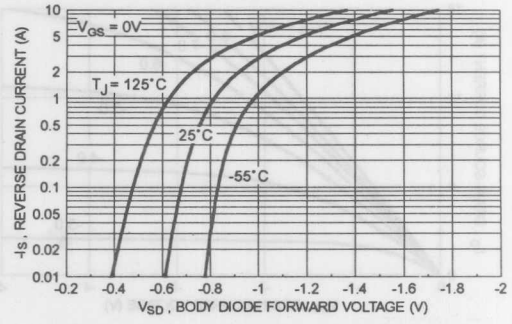


Figure 19. P-Channel Body Diode Forward Voltage Variation with Current and Temperature.

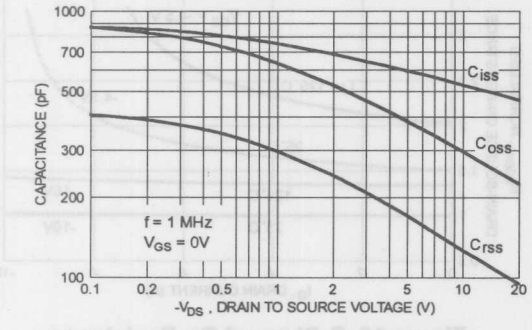


Figure 20. P-Channel Capacitance Characteristics.

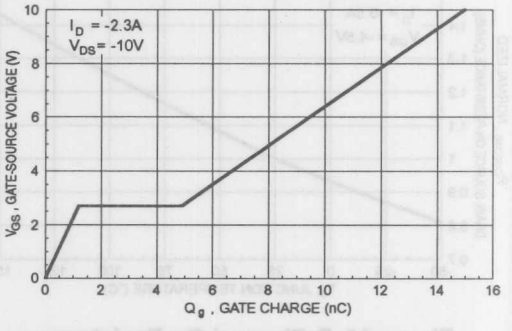


Figure 21. P-Channel Gate Charge Characteristic.

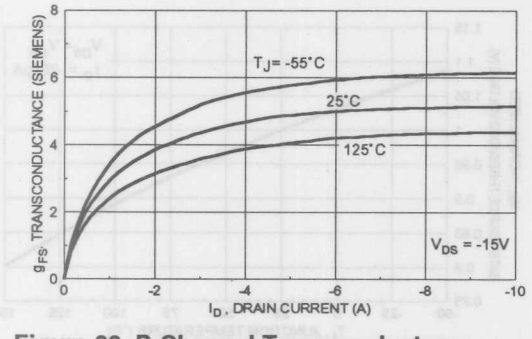


Figure 22. P-Channel Transconductance Variation with Drain Current and Temperature.

Typical Electrical Characteristic: N & P-Channel (continued)

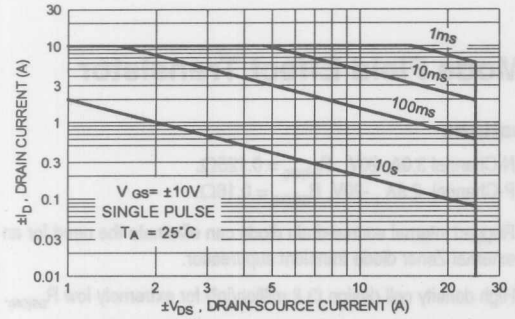


Figure 23. Maximum Safe Operating Area for both N & P-Channel.

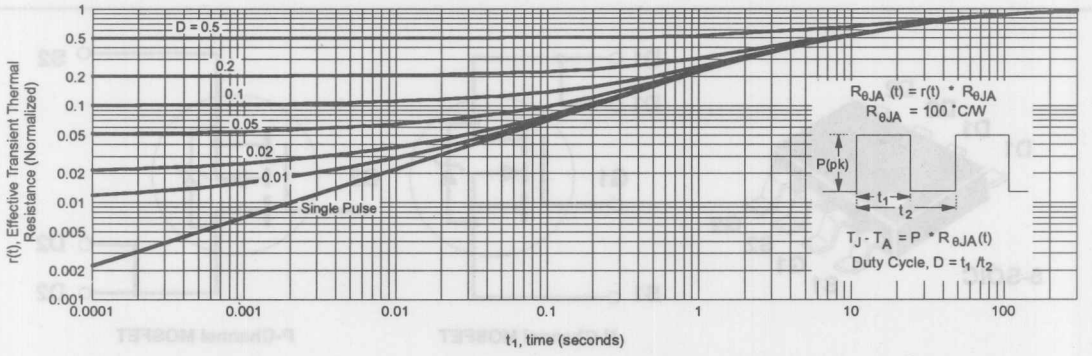


Figure 24. Transient Thermal Response Curve for N or P-Channel Surface-Mounted Device.

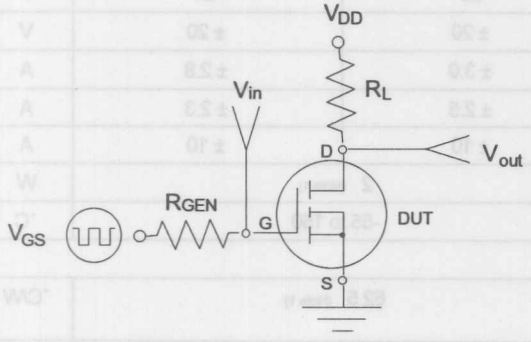


Figure 25. N or P-Channel Switching Test Circuit.

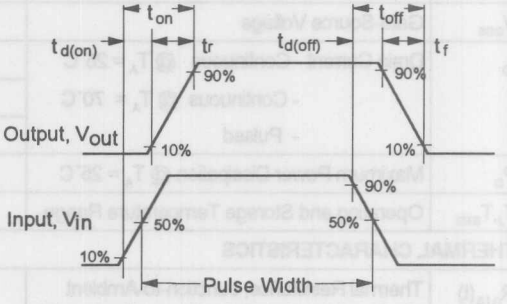


Figure 26. N or P-Channel Switching Waveforms.

National Semiconductor

July 1993

ADVANCE INFORMATION

NDS9943

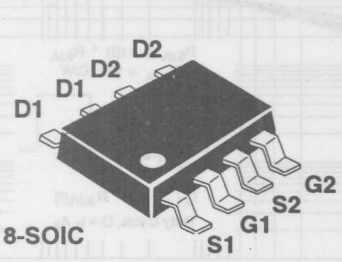
Dual N & P-Channel Enhancement Mode Field Effect Transistor

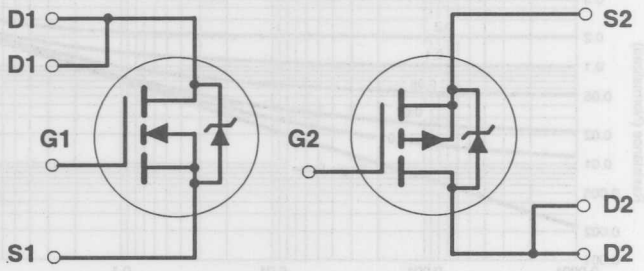
General Description

These dual n- and p-channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulses in the avalanche and commutation modes. These devices are particularly suited for low voltage applications such as laptop computer power management and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- N-Channel 3.0A, 20V, $R_{DS(ON)}$ = 0.125Ω.
  P-Channel -2.8A , -20V, $R_{DS(ON)}$ = 0.16Ω.
- Rugged internal source-drain diode can eliminate the need for an external Zener diode transient suppressor.
- High density cell design (3.8 million/in²) for extremely low $R_{DS(ON)}$.
- High power and current handling capability in a widely used surface mount package.
- Dual (N & P-Channel) MOSFET in surface mount package.
- Critical DC electrical parameters specified at elevated temperature.





N-Channel MOSFET P-Channel MOSFET

Absolute Maximum Ratings

T_C = 25°C unless otherwise noted

Symbol	Parameter	N-Channel	P-Channel	Units
V_{DSS}	Drain-Source Voltage	20	-20	V
V_{DGR}	Drain-Gate Voltage (R_{GS} ≤ 1 MΩ)	20	-20	V
V_{GSS}	Gate-Source Voltage	± 20	± 20	V
I_D	Drain Current - Continuous @ T_A = 25°C	± 3.0	± 2.8	A
	- Continuous @ T_A = 70°C	± 2.5	± 2.3	A
	- Pulsed	± 10	± 10	A
P_D	Maximum Power Dissipation @ T_A = 25°C	2 (Note 1)		W
T_J,T_{STG}	Operating and Storage Temperature Range	-55 to 150		°C
THERMAL CHARACTERISTICS				
$R_{\theta JA}(t)$	Thermal Resistance, Junction-to-Ambient (Surface Mounted. Pulse time = 10 seconds)	62.5 (Note 1)		°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Surface Mounted. Steady-State)	100		°C/W

Electrical Characteristics (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Type	Min	Typ	Max	Units
OFF CHARACTERISTICS							
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	N-Ch	20			V
		V_{GS} = 0 V, I_D = -250 µA	P-Ch	-20			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 16 V, V_{GS} = 0 V	N-Ch			2	µA
		T_C = 55°C				25	µA
		V_{DS} = -16 V, V_{GS} = 0 V	P-Ch			-2	µA
		T_C = 55°C				-25	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V				100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS} = 0 V				-100	nA
ON CHARACTERISTICS (Note 2)							
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	N-Ch	1	1.5	3	V
		T_C=125°C		0.7	1.1	2.2	V
		V_{DS} = V_{GS}, I_D = -250 µA	P-Ch	-1		-3	V
		T_C=125°C		TBD		TBD	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 3.0 A	N-Ch		0.062	0.125	Ω
		T_C=125°C			0.085	0.175	Ω
		V_{GS} = 6 V, I_D = 2.0 A			0.073	0.16	Ω
		V_{GS} = 4.5 V, I_D = 1.5 A			0.08	0.25	Ω
		T_C=125°C			0.11	0.35	Ω
		V_{GS} = -10 V, I_D = -3.0 A	P-Ch			0.16	Ω
		T_C=125°C				TBD	Ω
		V_{GS} = -6 V, I_D = -2.0 A				0.2	Ω
		V_{GS} = -4.5 V, I_D = -1.5 A				0.3	Ω
		T_C=125°C				TBD	Ω
$I_{D(on)}$	On-State Drain Current	V_{GS} = 10 V, V_{DS} = 5 V	N-Ch	10			A
		V_{GS} = 4.5 V, V_{DS} = 5 V		2			A
		V_{GS} = -10 V, V_{DS} = -5 V	P-Ch	-10			A
		V_{GS} = -4.5V, V_{DS} = -5 V		-2			A
g_{FS}	Forward Transconductance	V_{DS} = 15 V, I_D = 3.0 A	N-Ch		7		S
		V_{DS} = -15 V, I_D = -3.0 A	P-Ch		TBD		S
DYNAMIC CHARACTERISTICS							
C_{iss}	Input Capacitance	N-Channel V_{DS} = 10V, V_{GS} = 0 V, f = 1.0 MHz	N-Ch		525		pF
			P-Ch		TBD		pF
C_{oss}	Output Capacitance		N-Ch		315		pF
		P-Channel V_{DS} = -10 V, V_{GS} = 0 V, f = 1.0 MHz	P-Ch		TBD		pF
C_{rss}	Reverse Transfer Capacitance		N-Ch		185		pF
			P-Ch		TBD		pF

Electrical Characteristics (T_c = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Type	Min	Typ	Max	Units
SWITCHING CHARACTERISTICS (Note 2)							
$t_{D(ON)}$	Turn - On Delay Time	N-Channel V_{DD} = 20 V, I_D = 1 A, V_{GEN} = 10 V, R_{GEN} = 6 Ω	N-Ch		6	15	ns
			P-Ch			40	ns
t_r	Turn - On Rise Time		N-Ch		12	20	ns
		P-Channel V_{DD} = -20 V, I_D = -1 A, V_{GEN} = -10 V, R_{GEN} = 6 Ω	P-Ch			40	ns
$t_{D(OFF)}$	Turn - Off Delay Time		N-Ch		22	50	ns
			P-Ch			90	ns
t_f	Turn - Off Fall Time		N-Ch		8	50	ns
			P-Ch			50	ns
Q_g	Total Gate Charge	N-Channel V_{DS} = 10V, I_D = 2.3A, V_{GS} = 10 V	N-Ch		17	25	nC
			P-Ch		TBD	25	nC
Q_{gs}	Gate-Source Charge	P-Channel V_{DS} = -10V, I_D = -2.3A, V_{GS} = -10 V	N-Ch		1.2		nC
			P-Ch		TBD		nC
Q_{gd}	Gate-Drain Charge		N-Ch		5		nC
			P-Ch		TBD		nC
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS							
I_S	Maximum Continuous Drain-Source Diode Forward Current		N-Ch			1.6	A
			P-Ch			-1.6	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 1.25 A (Note 2)	N-Ch		0.78	1.2	V
		V_{GS} = 0 V, I_S = -1.25 A (Note 2)	P-Ch			-1.6	V
t_{rr}	Reverse Recovery Time	N-Channel V_{GS} = 0V, I_S = 1.25 A, dI_S/dt = 100 A/µs	N-Ch			100	ns
			P-Ch			100	ns
I_{rr}	Reverse Recovery Current	P-Channel V_{GS} = 0V, I_S = -1.25 A, dI_S/dt = 100 A/µs	N-Ch		TBD		A
			P-Ch		TBD		A

Notes:

1. Power dissipation and thermal resistance determinations based on an assumption that a 10 second pulse is equivalent to steady-state.
2. Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics: N-Channel

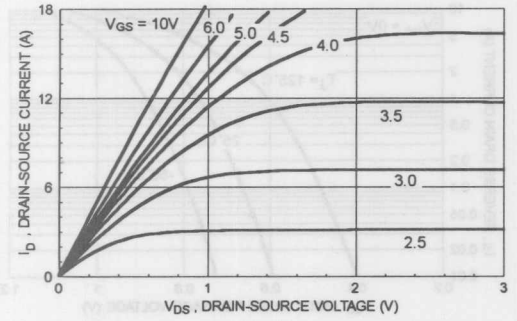


Figure 1. On-Region Characteristics.

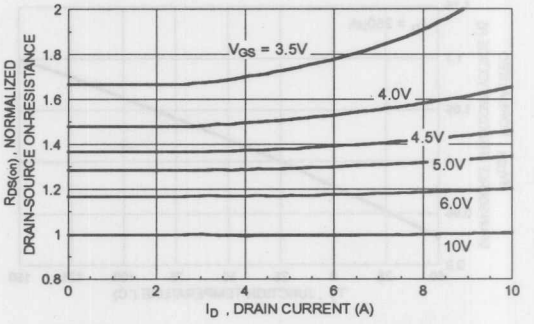


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current.

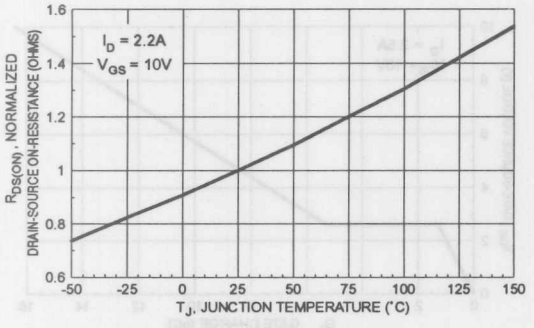


Figure 3. On-Resistance Variation with Temperature.

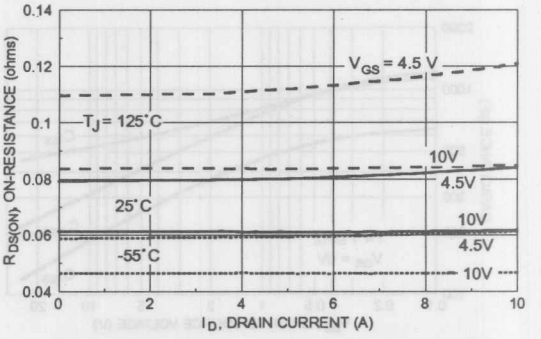


Figure 4. On-Resistance Variation with Drain Current and Temperature.

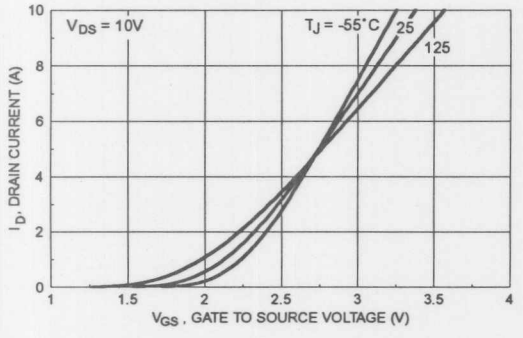


Figure 5. Transfer Characteristics.

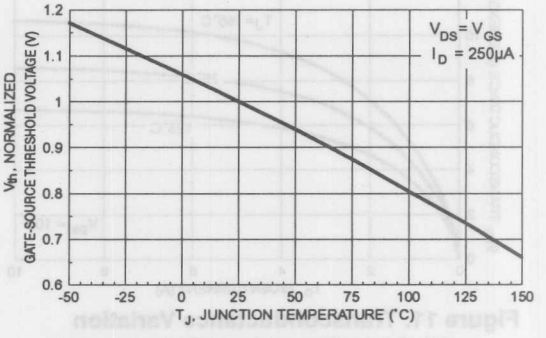


Figure 6. Gate Threshold Variation with Temperature.

Typical Electrical Characteristics: N-Channel (continued)

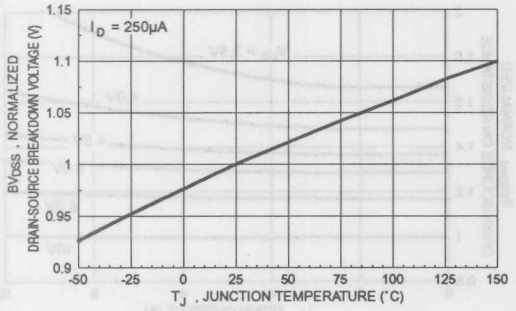


Figure 7. Breakdown Voltage Variation with Temperature.

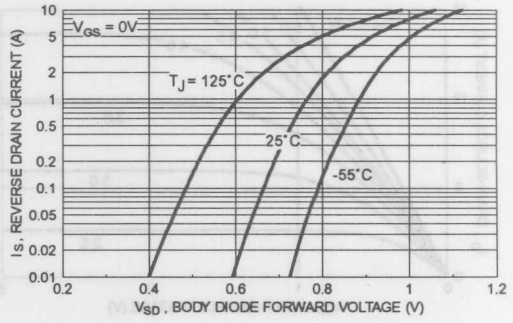


Figure 8. Body Diode Forward Voltage Variation with Current and Temperature

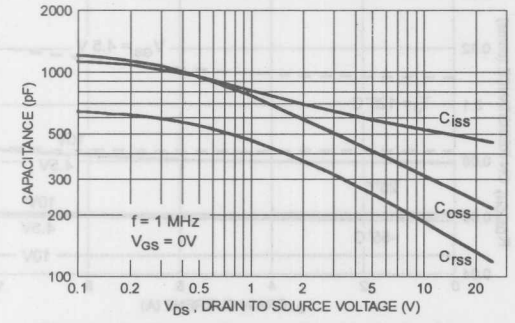


Figure 9. Capacitance Characteristics.

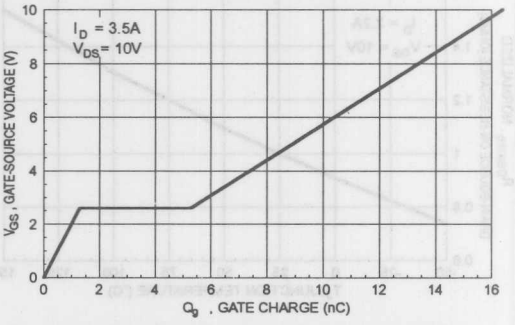


Figure 10. Gate Charge Characteristics.

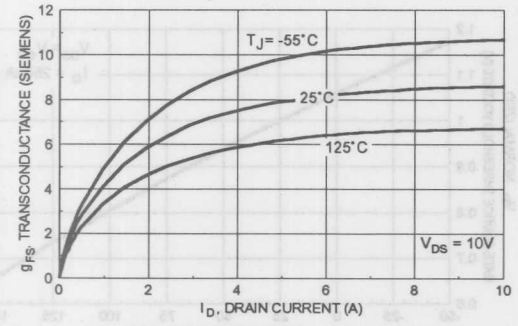


Figure 11. Transconductance Variation with Drain Current and Temperature.

Typical Electrical Characteristic: N & P-Channel (continued)

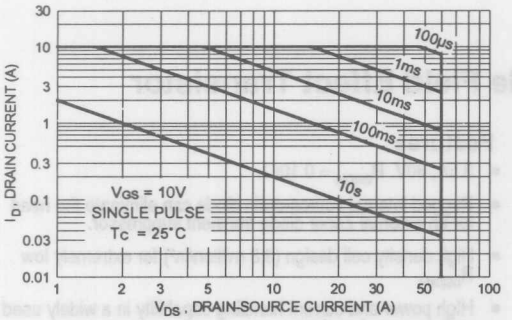


Figure 12. Maximum Safe Operating Area.

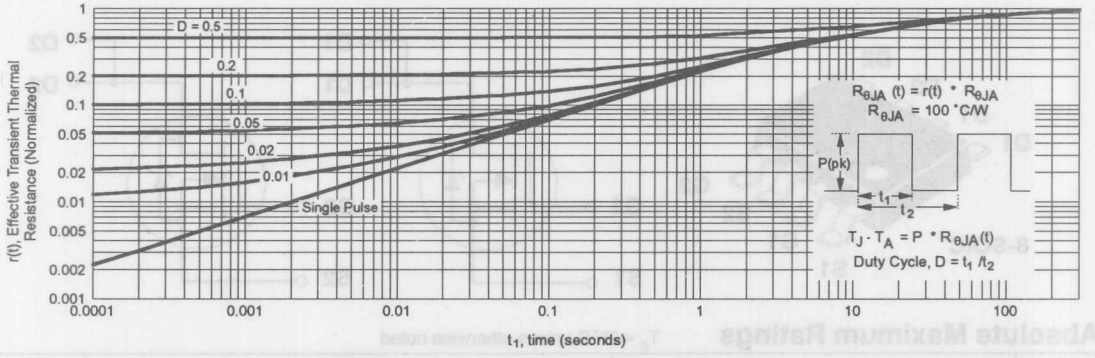


Figure 13. Transient Thermal Response Curve for Surface-Mounted Device.

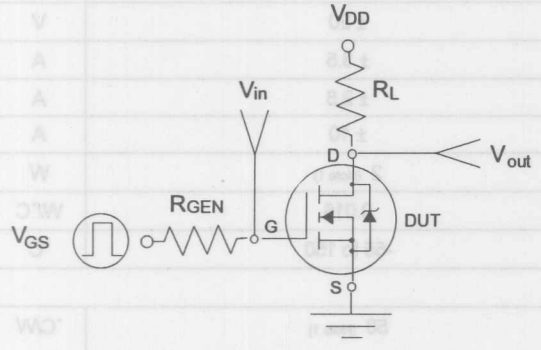


Figure 14. Switching Test Circuit

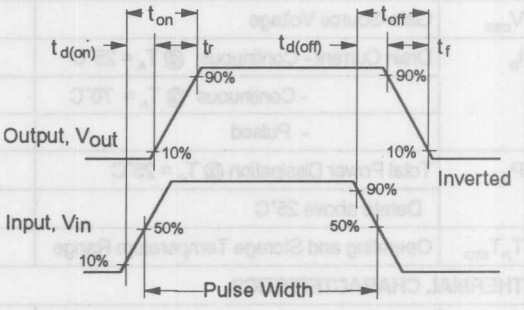


Figure 15. Switching Waveforms

National Semiconductor

May 1993

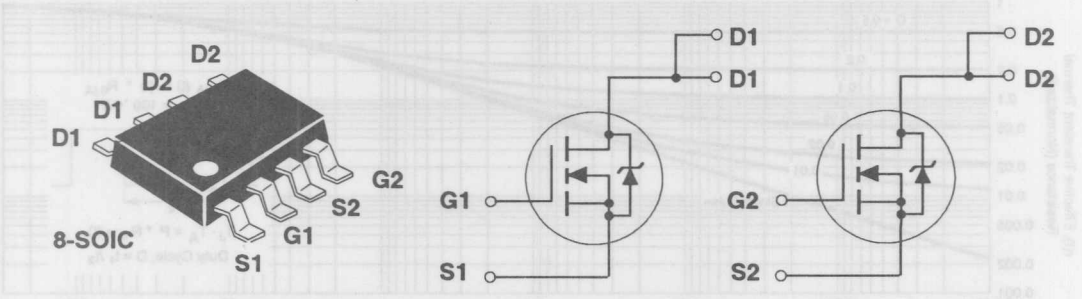
NDS9945
Dual N-Channel Enhancement Mode Field Effect Transistor

General Description

These n-channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulses in the avalanche and commutation modes. These devices are particularly suited for low voltage applications such as laptop computer power management and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- 3.5A, 60V. $R_{DS(ON)} = 0.10\Omega$.
- Rugged internal source-drain diode can eliminate the need for an external Zener diode transient suppressor.
- High density cell design (3.8 million/in²) for extremely low $R_{DS(ON)}$.
- HIgh power and current handling capability in a widely used surface mount package.
- Dual MOSFET in surface mount package.
- Critical DC electrical parameters specified at elevated temperature.



Absolute Maximum Ratings

$T_C = 25^\circ C$ unless otherwise noted

Symbol	Parameter	NDS9945	Units
V_{DSS}	Drain-Source Voltage	60	V
V_{DGR}	Drain-Gate Voltage ($R_{GS} \leq 1$ MΩ)	60	V
V_{GSS}	Gate-Source Voltage	± 20	V
I_D	Drain Current - Continuous @ $T_A = 25^\circ C$	± 3.5	A
	- Continuous @ $T_A = 70^\circ C$	± 2.8	A
	- Pulsed	± 10	A
P_D	Total Power Dissipation @ $T_C = 25^\circ C$	2 (Note 1)	W
	Derate above 25°C	0.016	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to 150	°C
THERMAL CHARACTERISTICS			
$R_{\theta JA}(t)$	Thermal Resistance, Junction to Ambient (Surface Mounted. Pulse time = 10 seconds)	50 (Note 1)	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Surface Mounted. Steady-State)	100	°C/W

Electrical Characteristics (T_c = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	60			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 48 V, V_{GS} = 0 V			1	µA
		V_{DS} = 48 V, V_{GS} = 0 V, T_c = 55°C			25	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	1	1.5	3	V
		V_{DS} = V_{GS}, I_D = 250 µA, T_c=125°C	0.7		2.2	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 3.5 A		0.084	0.1	Ω
		V_{GS} = 10 V, I_D = 3.5 A, T_c=125°C		0.13	0.2	Ω
		V_{GS} = 4.5 V, I_D = 2.5 A		0.11	0.2	Ω
		V_{GS} = 4.5 V, I_D = 2.5 A, T_c=125°C		0.17	0.3	Ω
$I_{D(on)}$	On-State Drain Current	V_{GS} = 10 V, V_{DS} = 10 V	10			A
		V_{GS} = 4.5 V, V_{DS} = 10 V	3.5			A
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 3.5 A	4	6.3		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz		435		pF
C_{oss}	Output Capacitance			120		pF
C_{rss}	Reverse Transfer Capacitance			30		pF
SWITCHING CHARACTERISTICS (Note 2)						
$t_{D(ON)}$	Turn - On Delay Time	V_{DD} = 30V, I_D = 1 A, V_{GS} = 10 V, R_{GEN} = 6 Ω		8		ns
t_r	Turn - On Rise Time			4		ns
$t_{D(OFF)}$	Turn - Off Delay Time			24		ns
t_f	Turn - Off Fall Time			7		ns
Q_g	Total Gate Charge	V_{DS} = 30 V, I_D = 3.5 A, V_{GS} = 10 V		13	30	nC
Q_{gs}	Gate-Source Charge			1.2		nC
Q_{gd}	Gate-Drain Charge			4.7		nC
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuos Drain-Source Diode Forward Current				1.7	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 1.7 A (Note 2)		0.8	1.2	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0V, I_S = 1.7 A, dI_S/dt = 100 A/µs		52		ns
I_{rr}	Reverse Recovery Current			2.3		A

Notes:

1. Power dissipation and thermal resistance determinations based on an assumption that a 10 second pulse is equivalent to steady-state.
2. Pulse Test: Pulse Width ≤ 300 ms, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

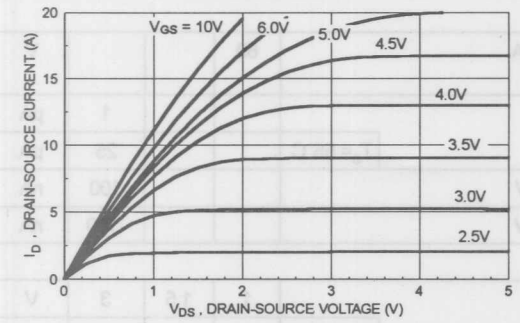


Figure 1. On-Region Characteristics.

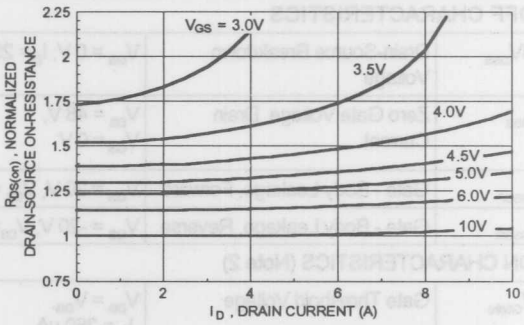


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current.

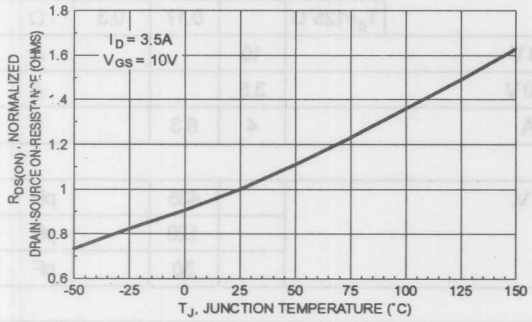


Figure 3. On-Resistance Variation with Temperature.

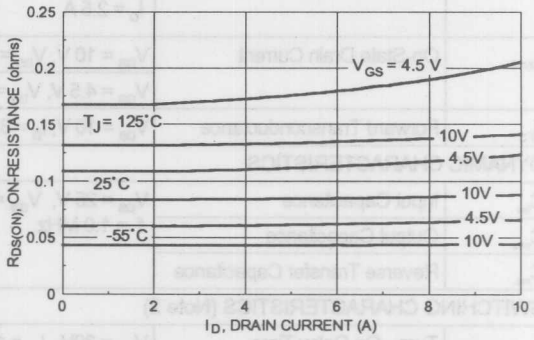


Figure 4. On-Resistance Variation with Drain Current and Temperature.

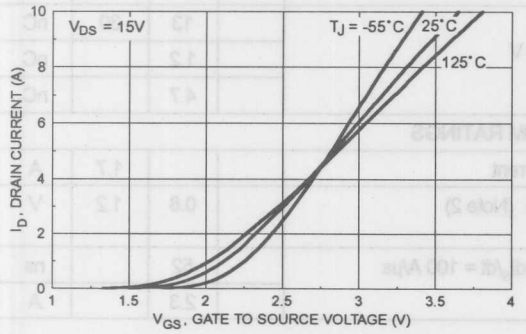


Figure 5. Transfer Characteristics.

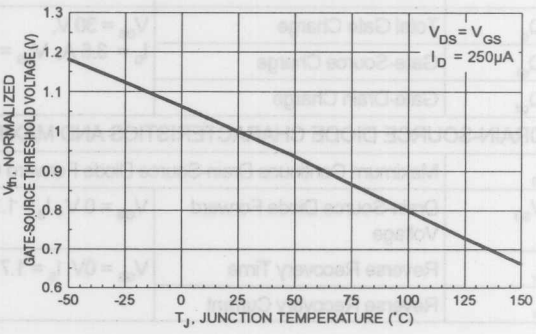


Figure 6. Gate Threshold Variation with Temperature.

Typical Electrical Characteristics (continued)

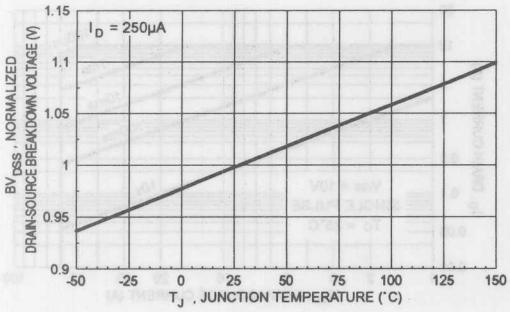


Figure 7. Breakdown Voltage Variation with Temperature.

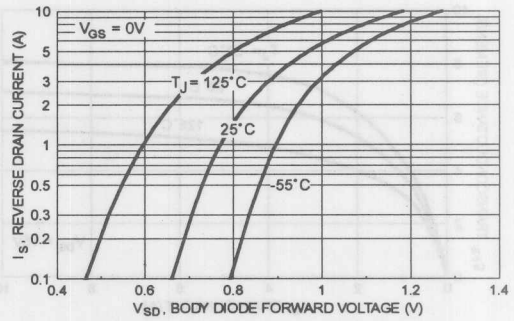


Figure 8. Body Diode Forward Voltage Variation with Current and Temperature

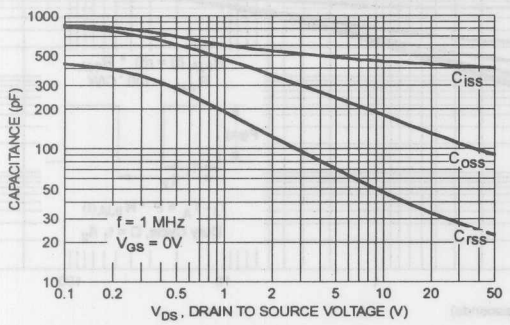


Figure 9. Capacitance Characteristics.

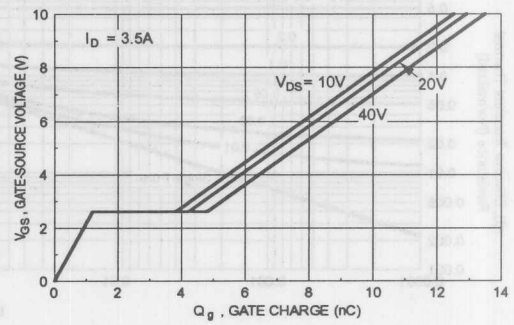


Figure 10. Gate Charge Characteristics.

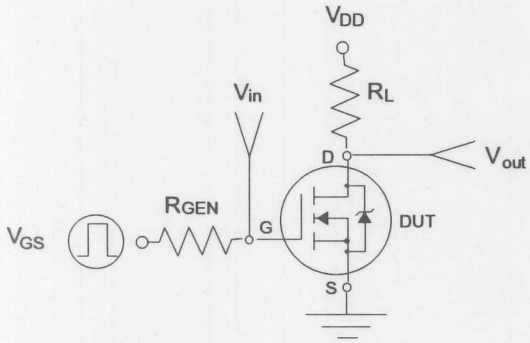


Figure 11. Switching Test Circuit

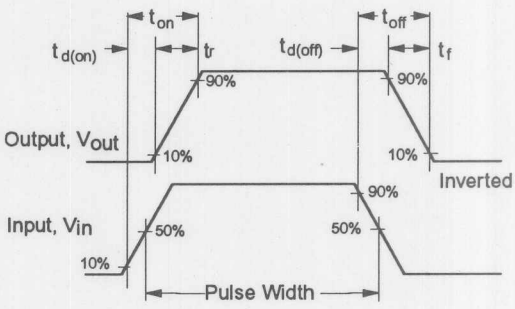


Figure 12. Switching Waveforms

Typical Electrical Characteristics (continued)

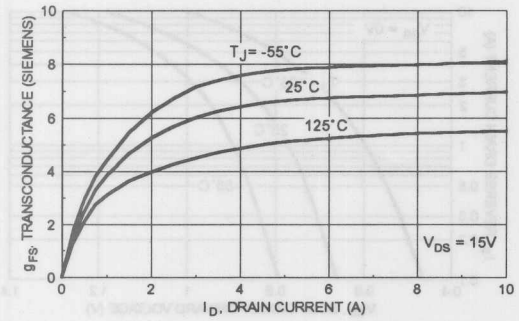


Figure 13. Transconductance Variation with Drain Current and Temperature.

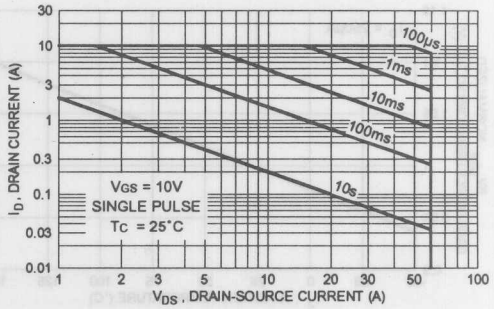


Figure 14. Maximum Safe Operating Area.

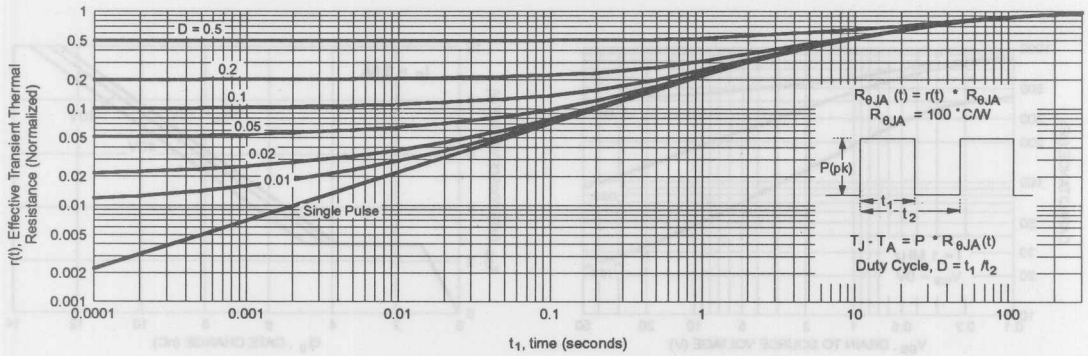


Figure 17. Transient Thermal Response Curve.

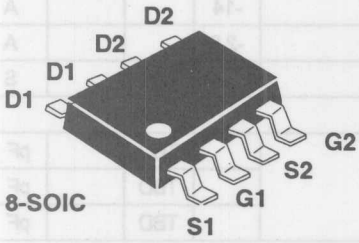
NDS9947
Dual P-Channel Enhancement Mode Field Effect Transistor

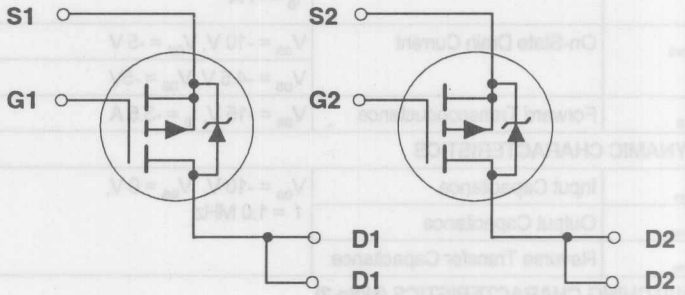
General Description

These p-channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulses in the avalanche and commutation modes. These devices are particularly suited for low voltage applications such as laptop computer power management and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- 3.5A, -20V. $R_{DS(ON)}$ = 0.11Ω.
- Rugged internal source-drain diode can eliminate the need for an external Zener diode transient suppressor.
- High density cell design (3.8 million/in²) for extremely low $R_{DS(ON)}$.
- HIgh power and current handling capability in a widely used surface mount package.
- Dual MOSFET in surface mount package.
- Critical DC electrical parameters specified at elevated temperature.





Absolute Maximum Ratings

T_C = 25°C unless otherwise noted

Symbol	Parameter		NDS9947	Units
V_{DSS}	Drain-Source Voltage		-20	V
V_{DGR}	Drain-Gate Voltage ($R_{GS} \leq 1$ MΩ)		-20	V
V_{GSS}	Gate-Source Voltage		± 20	V
I_D	Drain Current - Continuous	T_A = 25°C	± 3.5	A
	- Pulsed		± 10	A
	Drain Current - Continuous	T_A = 70°C	± 2.5	A
P_D	Maximum Power Dissipation	T_A = 25°C	2 (Note 1)	W
		T_A = 70°C	1.3 (Note 1)	W
T_J,T_{STG}	Operating and Storage Temperature Range		-55 to 150	°C
THERMAL CHARACTERISTICS				
$R_{\theta JA}$(t)	Thermal Resistance, Junction-to-Ambient (Surface Mounted. Pulse time = 10 seconds)		62.5 (Note 1)	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Surface Mounted. Steady-State)		100	°C/W

Electrical Characteristics (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = -250 µA	-20			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -16 V, V_{GS} = 0 V			-1	µA
		T_C = 55°C			-10	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = -250 µA	-1		-3	V
		T_C=125°C	TBD		TBD	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = -10 V, I_D = -3.5 A			0.11	Ω
		T_C=125°C			TBD	Ω
		V_{GS} = -4.5 V, I_D = -1 A			0.19	Ω
		T_C=125°C			TBD	Ω
$I_{D(on)}$	On-State Drain Current	V_{GS} = -10 V, V_{DS} = -5 V	-14			A
		V_{GS} = -4.5 V, V_{DS} = -5V	-2.5			A
g_{FS}	Forward Transconductance	V_{DS} = -15 V, I_D = -3.5 A		TBD		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = -10 V, V_{GS} = 0 V, f = 1.0 MHz		TBD		pF
C_{oss}	Output Capacitance			TBD		pF
C_{rss}	Reverse Transfer Capacitance			TBD		pF
SWITCHING CHARACTERISTICS (Note 2)						
$t_{D(ON)}$	Turn - On Delay Time	V_{DD} = -10 V, I_D = -1 A, V_{GEN} = -10 V, R_{GEN} = 6 Ω			TBD	ns
t_r	Turn - On Rise Time				TBD	ns
$t_{D(OFF)}$	Turn - Off Delay Time				TBD	ns
t_f	Turn - Off Fall Time				TBD	ns
Q_g	Total Gate Charge	V_{DS} = -10 V, I_D = -3.5 A, V_{GS} = -10 V		TBD		nC
Q_{gs}	Gate-Source Charge			TBD		nC
Q_{gd}	Gate-Drain Charge			TBD		nC
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain-Source Diode Forward Current				-3.5	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = -3.5 A (Note 2)			-1.2	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0V, I_S = 3.5 A, dI_S/dt = 100 A/µs			100	ns
I_{rr}	Reverse Recovery Current			TBD		A

Notes:

1. Power dissipation and thermal resistance determinations based on an assumption that a 10 second pulse is equivalent to steady-state.
2. Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%.

National Semiconductor

July 1993

ADVANCE INFORMATION

NDS9948

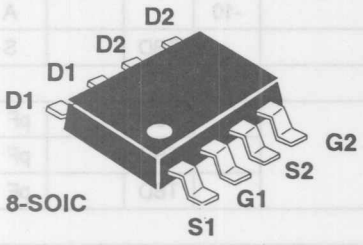
Dual P-Channel Enhancement Mode Field Effect Transistor

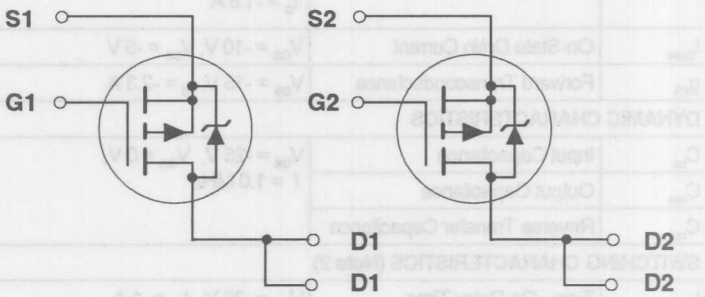
General Description

These p-channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulses in the avalanche and commutation modes. These devices are particularly suited for low voltage applications such as laptop computer power management and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- 2.3A, -60V. $R_{DS(ON)}$ = 0.25Ω.
- Rugged internal source-drain diode can eliminate the need for an external Zener diode transient suppressor.
- High density cell design (3.8 million/in²) for extremely low $R_{DS(ON)}$.
- HIgh power and current handling capability in a widely used surface mount package.
- Dual MOSFET in surface mount package.
- Critical DC electrical parameters specified at elevated temperature.





Absolute Maximum Ratings

T_C = 25°C unless otherwise noted

Symbol	Parameter	NDS9948	Units
V_{DSS}	Drain-Source Voltage	-60	V
V_{DGR}	Drain-Gate Voltage ($R_{GS} \leq 1$ MΩ)	-60	V
V_{GSS}	Gate-Source Voltage	± 20	V
I_D	Drain Current - Continuous T_A = 25°C	± 2.3	A
	- Pulsed	± 10	A
	Drain Current - Continuous T_A = 70°C	± 1.8	A
P_D	Maximum Power Dissipation T_A = 25°C	2 (Note 1)	W
	T_A = 70°C	1.3 (Note 1)	W
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to 150	°C
THERMAL CHARACTERISTICS			
$R_{\theta JA}(t)$	Thermal Resistance, Junction-to-Ambient (Surface Mounted. Pulse time = 10 seconds)	62.5 (Note 1)	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Surface Mounted. Steady-State)	100	°C/W

Electrical Characteristics (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
OFF CHARACTERISTICS							
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = -250 µA		-60			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -40 V, V_{GS} = 0 V				-2	µA
			T_C = 55°C			-25	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V				100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS} = 0 V				-100	nA
ON CHARACTERISTICS (Note 2)							
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = -250 µA		-1		-3	V
			T_C=125°C	TBD		TBD	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = -10 V, I_D = -2.3 A				0.25	Ω
			T_C=125°C			TBD	Ω
		V_{GS} = -4.5 V, I_D = -1.6 A				0.5	Ω
			T_C=125°C			TBD	Ω
$I_{D(on)}$	On-State Drain Current	V_{GS} = -10 V, V_{DS} = -5 V		-10			A
g_{FS}	Forward Transconductance	V_{DS} = -15 V, I_D = -2.3 A			TBD		S
DYNAMIC CHARACTERISTICS							
C_{iss}	Input Capacitance	V_{DS} = -25 V, V_{GS} = 0 V, f = 1.0 MHz			TBD		pF
C_{oss}	Output Capacitance				TBD		pF
C_{rss}	Reverse Transfer Capacitance				TBD		pF
SWITCHING CHARACTERISTICS (Note 2)							
$t_{D(ON)}$	Turn - On Delay Time	V_{DD} = -30 V, I_D = -1 A, V_{GEN} = -10 V, R_{GEN} = 6 Ω				TBD	ns
t_r	Turn - On Rise Time					TBD	ns
$t_{D(OFF)}$	Turn - Off Delay Time					TBD	ns
t_f	Turn - Off Fall Time					TBD	ns
Q_g	Total Gate Charge	V_{DS} = -30 V, I_D = -2.3 A, V_{GS} = -10 V			TBD		nC
Q_{gs}	Gate-Source Charge				TBD		nC
Q_{gd}	Gate-Drain Charge				TBD		nC
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS							
I_S	Maximum Continuous Drain-Source Diode Forward Current					-2.3	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = -2.3 A (Note 2)				-1.2	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0V, I_S = 2.3 A, dI_S/dt = 100 A/µs			TBD		ns
I_{rr}	Reverse Recovery Current				TBD		A

Notes:
1. Power dissipation and thermal resistance determinations based on an assumption that a 10 second pulse is equivalent to steady-state.
2. Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%.

National Semiconductor

August 1993

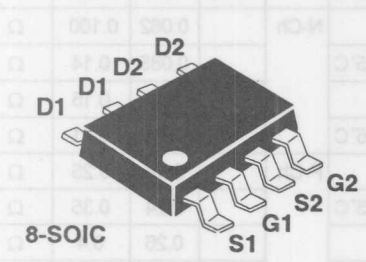
NDS9952
Dual N & P-Channel Enhancement Mode Field Effect Transistor

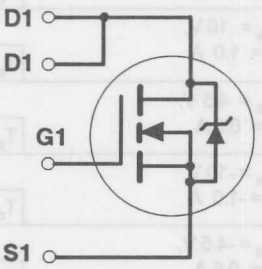
General Description

These dual n- and p-channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulses in the avalanche and commutation modes. These devices are particularly suited for low voltage applications such as laptop computer power management and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

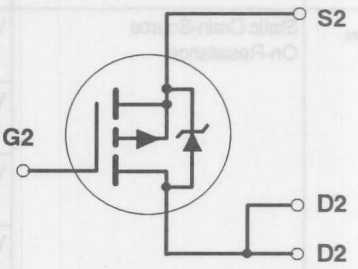
Features

- N-Channel 3.5A, 25V, $R_{DS(ON)}$ = 0.100Ω.
  P-Channel -2.3A , -25V, $R_{DS(ON)}$ = 0.25Ω.
- Rugged internal source-drain diode can eliminate the need for an external Zener diode transient suppressor.
- High density cell design (3.8 million/in²) for extremely low $R_{DS(ON)}$.
- High power and current handling capability in a widely used surface mount package.
- Dual (N & P-Channel) MOSFET in surface mount package.
- Critical DC electrical parameters specified at elevated temperature.





N-Channel MOSFET



P-Channel MOSFET

Absolute Maximum Ratings

T_C = 25°C unless otherwise noted

Symbol	Parameter	N-Channel	P-Channel	Units
V_{DSS}	Drain-Source Voltage	25	-25	V
V_{DGR}	Drain-Gate Voltage ($R_{GS} \leq 1$ MΩ)	25	-25	V
V_{GSS}	Gate-Source Voltage	± 20	± 20	V
I_D	Drain Current - Continuous @ T_A = 25°C	± 3.5	± 2.3	A
	- Continuous @ T_A = 70°C	± 2.8	± 1.9	A
	- Pulsed	± 14	± 9.2	A
P_D	Maximum Power Dissipation @ T_A = 25°C	2 (Note 1)		W
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to 150		°C
THERMAL CHARACTERISTICS				
$R_{\theta JA}(t)$	Thermal Resistance, Junction-to-Ambient (Surface Mounted. Pulse time = 10 seconds)	62.5 (Note 1)		°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Surface Mounted. Steady-State)	100		°C/W

Electrical Characteristics (T_c = 25°C unless otherwise noted)

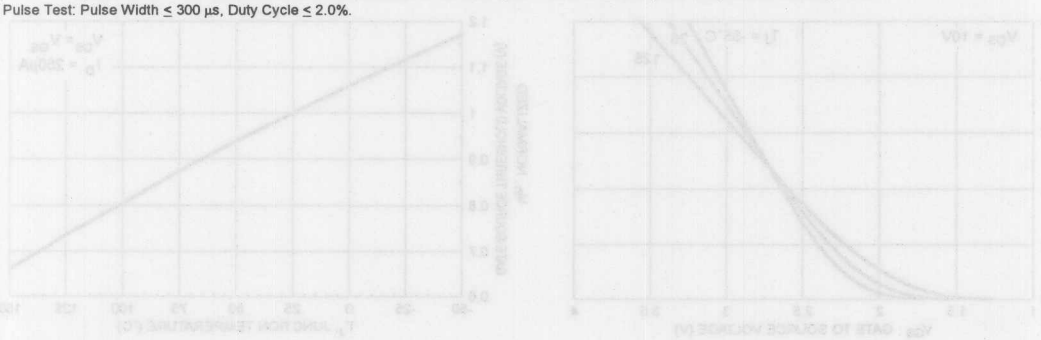
Symbol	Parameter	Conditions	Type	Min	Typ	Max	Units
OFF CHARACTERISTICS							
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	N-Ch	25			V
		V_{GS} = 0 V, I_D = -250 µA	P-Ch	-25			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 20 V, V_{GS} = 0 V	N-Ch			2	µA
		V_{DS} = 20 V, V_{GS} = 0 V, T_c = 55°C	N-Ch			25	µA
		V_{DS} = -20 V, V_{GS} = 0 V	P-Ch			-2	µA
		V_{DS} = -20 V, V_{GS} = 0 V, T_c = 55°C	P-Ch			-25	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V				100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS} = 0 V				-100	nA
ON CHARACTERISTICS (Note 2)							
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	N-Ch	1	1.5	3	V
		V_{DS} = V_{GS}, I_D = 250 µA, T_c=125°C	N-Ch	0.7	1.1	2.2	V
		V_{DS} = V_{GS}, I_D = -250 µA	P-Ch	-1	-2	-3	V
		V_{DS} = V_{GS}, I_D = -250 µA, T_c=125°C	P-Ch	-0.85	-1.7	-2.6	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 1.0 A	N-Ch		0.062	0.100	Ω
		V_{GS} = 10 V, I_D = 1.0 A, T_c=125°C	N-Ch		0.085	0.14	Ω
		V_{GS} = 4.5 V, I_D = 0.5 A	N-Ch		0.08	0.15	Ω
		V_{GS} = 4.5 V, I_D = 0.5 A, T_c=125°C	N-Ch		0.11	0.21	Ω
		V_{GS} = -10 V, I_D = -1.0 A	P-Ch		0.18	0.25	Ω
		V_{GS} = -10 V, I_D = -1.0 A, T_c=125°C	P-Ch		0.24	0.35	Ω
		V_{GS} = -4.5 V, I_D = -0.5 A	P-Ch		0.26	0.4	Ω
		V_{GS} = -4.5 V, I_D = -0.5 A, T_c=125°C	P-Ch		0.35	0.56	Ω
$I_{D(on)}$	On-State Drain Current	V_{GS} = 10 V, V_{DS} = 5 V	N-Ch	14			A
		V_{GS} = -10 V, V_{DS} = -5 V	P-Ch	-10			A
g_{FS}	Forward Transconductance	V_{DS} = 15 V, I_D = 3.5 A	N-Ch		7		S
		V_{DS} = -15 V, I_D = -3.5 A	P-Ch		3.8		S
DYNAMIC CHARACTERISTICS							
C_{iss}	Input Capacitance	N-Channel V_{DS} = 10V, V_{GS} = 0 V, f = 1.0 MHz	N-Ch		525		pF
			P-Ch		525		pF
C_{oss}	Output Capacitance		N-Ch		315		pF
		P-Channel V_{DS} = -10 V, V_{GS} = 0 V, f = 1.0 MHz	P-Ch		300		pF
C_{rss}	Reverse Transfer Capacitance		N-Ch		185		pF
			P-Ch		130		pF

Electrical Characteristics (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Type	Min	Typ	Max	Units
SWITCHING CHARACTERISTICS (Note 2)							
$t_{D(ON)}$	Turn - On Delay Time	N-Channel V_{DD} = 10 V, I_D = 1 A, V_{GEN} = 10 V, R_{GEN} = 6 Ω	N-Ch		6	15	ns
			P-Ch		8	40	ns
t_r	Turn - On Rise Time		N-Ch		12	20	ns
		P-Channel V_{DD} = -10 V, I_D = -1 A, V_{GEN} = -10 V, R_{GEN} = 6 Ω	P-Ch		15	40	ns
$t_{D(OFF)}$	Turn - Off Delay Time		N-Ch		22	50	ns
			P-Ch		25	90	ns
t_f	Turn - Off Fall Time		N-Ch		8	50	ns
			P-Ch		8	50	ns
Q_g	Total Gate Charge	N-Channel V_{DS} = 10V, I_D = 2.3A, V_{GS} = 10 V	N-Ch		17	27	nC
			P-Ch		15	25	nC
Q_{gs}	Gate-Source Charge		N-Ch		1.2		nC
		P-Channel V_{DS} = -10V, I_D = -2.3A, V_{GS} = -10 V	P-Ch		1.2		nC
Q_{gd}	Gate-Drain Charge		N-Ch		5		nC
			P-Ch		4.8		nC
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS							
I_S	Maximum Continuous Drain-Source Diode Forward Current		N-Ch			1.7	A
			P-Ch			-1.6	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 1.25 A (Note 2)	N-Ch		0.78	1.4	V
		V_{GS} = 0 V, I_S = -1.25 A (Note 2)	P-Ch		-0.94	-1.6	V
t_{rr}	Reverse Recovery Time	N-Channel V_{GS} = 0V, I_S = 1.25 A, dI_S/dt = 100 A/µs	N-Ch		28	75	ns
			P-Ch		29	100	ns
I_{rr}	Reverse Recovery Current	P-Channel V_{GS} = 0V, I_S = -1.25 A, dI_S/dt = 100 A/µs	N-Ch		2.1		A
			P-Ch		1.9		A

Notes:

1. Power dissipation and thermal resistance determinations based on an assumption that a 10 second pulse is equivalent to steady-state.
2. Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%.



Typical Electrical Characteristics: N-Channel

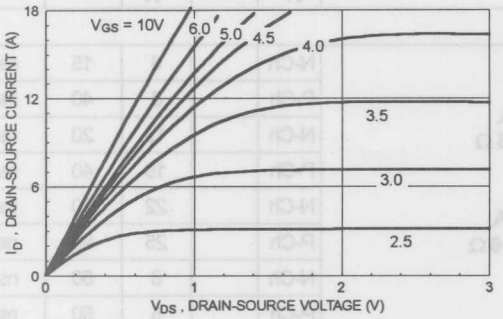


Figure 1. N-Channel On-Region Characteristic.

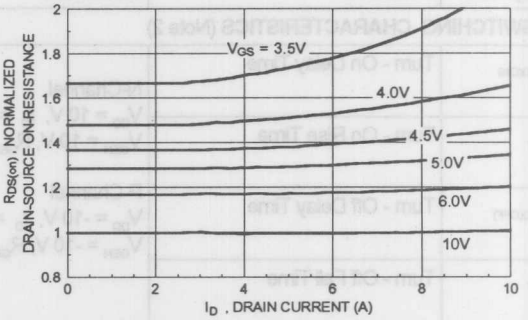


Figure 2. N-Channel On-Resistance Variation with Gate Voltage and Drain Current.

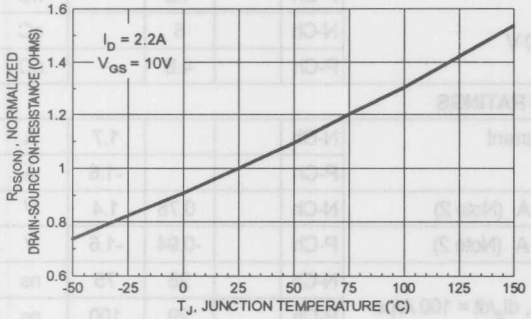


Figure 3. N-Channel On-Resistance Variation with Temperature.

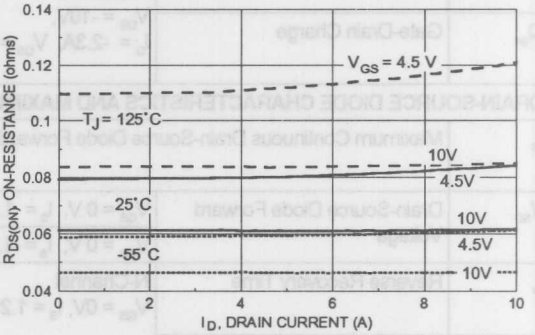


Figure 4. N-Channel On-Resistance Variation with Drain Current and Temperature.

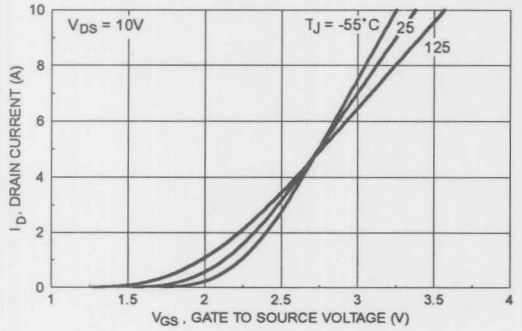


Figure 5. N-Channel Transfer Characteristic.

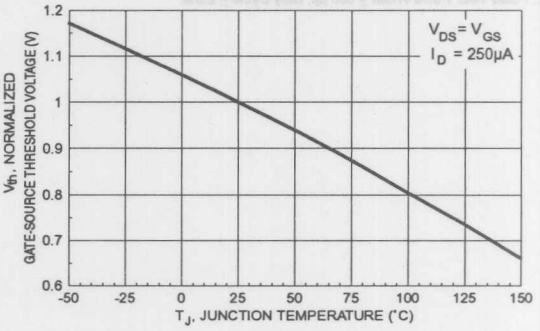


Figure 6. N-Channel Gate Threshold Variation with Temperature.

Typical Electrical Characteristics: N-Channel (continued)

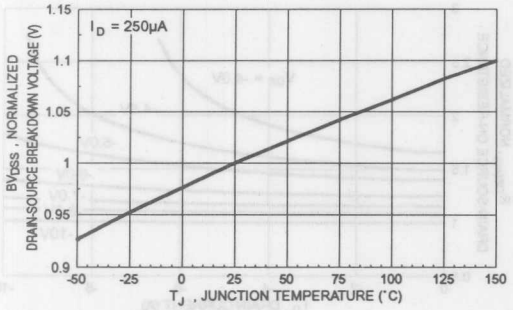


Figure 7. N-Channel Breakdown Voltage Variation with Temperature.

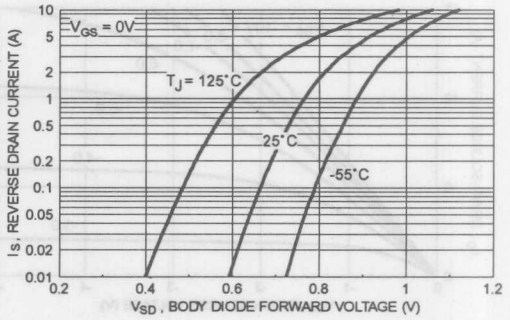


Figure 8. N-Channel Body Diode Forward Voltage Variation with Current and Temperature.

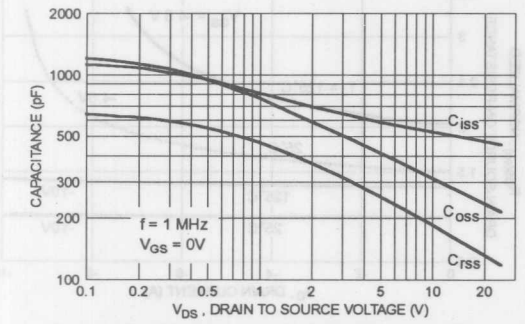


Figure 9. N-Channel Capacitance Characteristics.

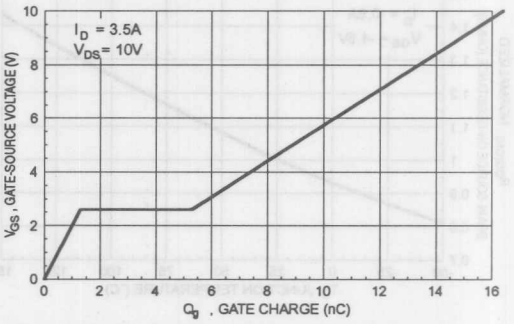


Figure 10. N-Channel Gate Charge Characteristic.

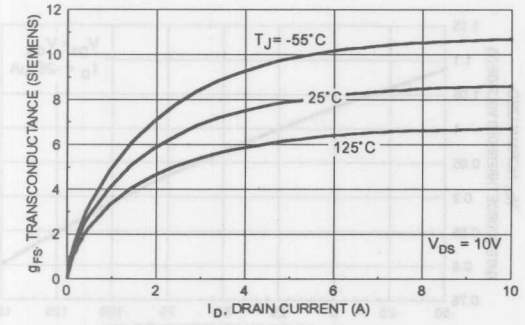


Figure 11. N-Channel Transconductance Variation with Drain Current and Temperature.

Typical Electrical Characteristics: P-Channel (continued)

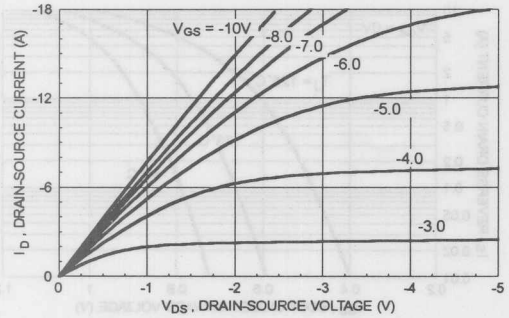


Figure 12. P-Channel On-Region Characteristics.

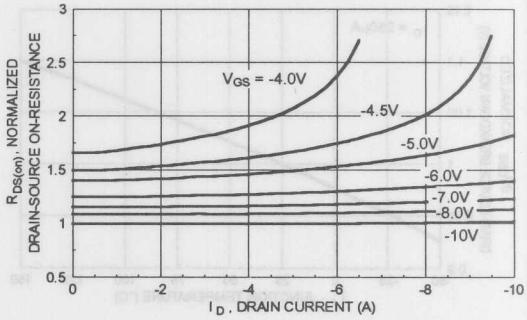


Figure 13. P-Channel On-Resistance Variation with Gate Voltage and Drain Current.

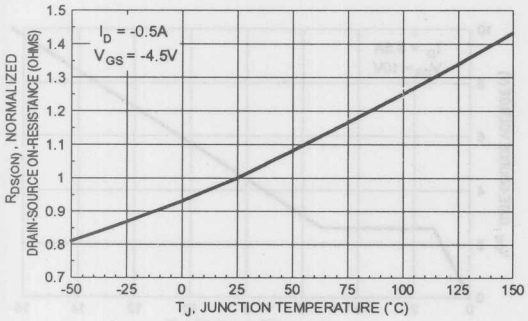


Figure 14. P-Channel On-Resistance Variation with Temperature.

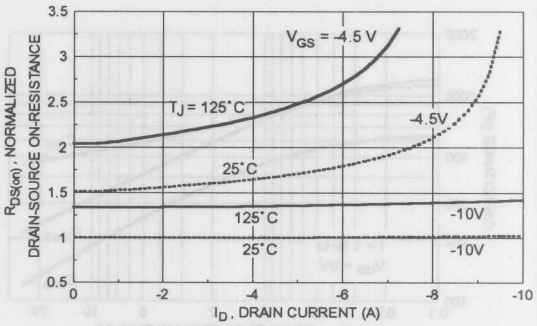


Figure 15. P-Channel On-Resistance Variation with Drain Current and Temperature.

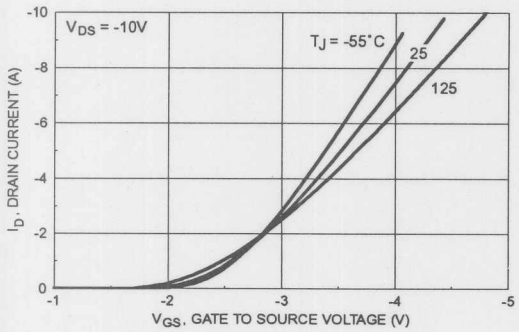


Figure 16. P-Channel Transfer Characteristics.

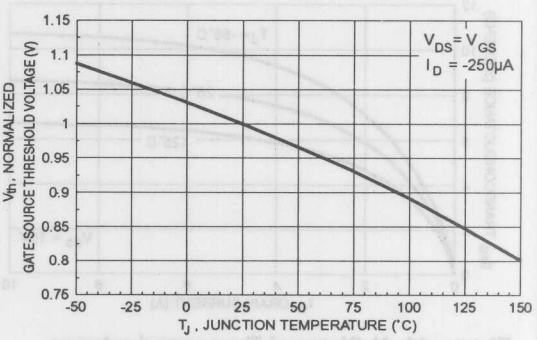


Figure 17. P-Channel Gate Threshold Variation with Temperature.

Typical Electrical Characteristics: P-Channel (continued)

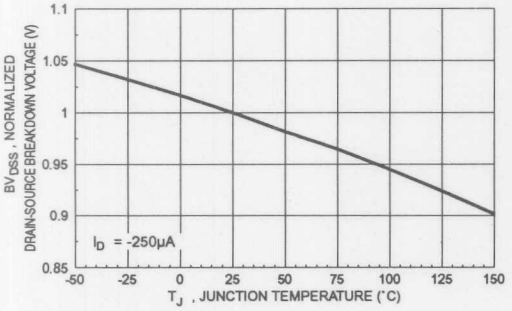


Figure 18. P-Channel Breakdown Voltage Variation with Temperature.

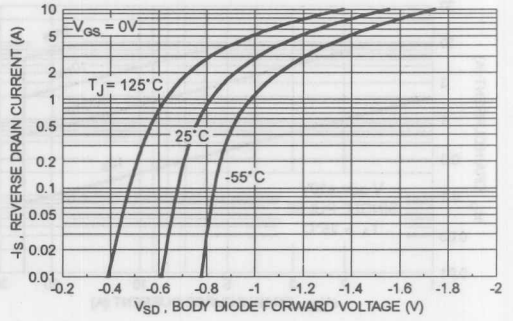


Figure 19. P-Channel Body Diode Forward Voltage Variation with Current and Temperature.

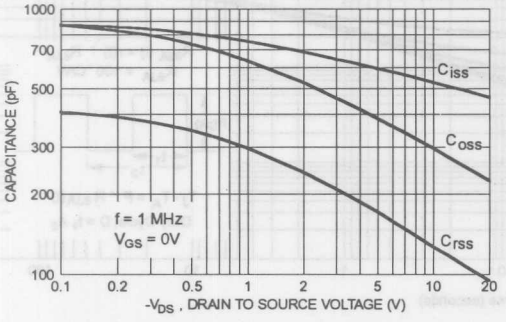


Figure 20. P-Channel Capacitance Characteristics.

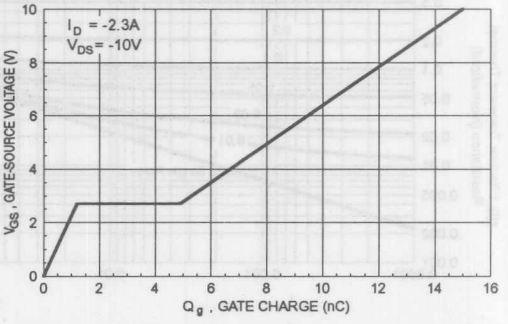


Figure 21. P-Channel Gate Charge Characteristic.

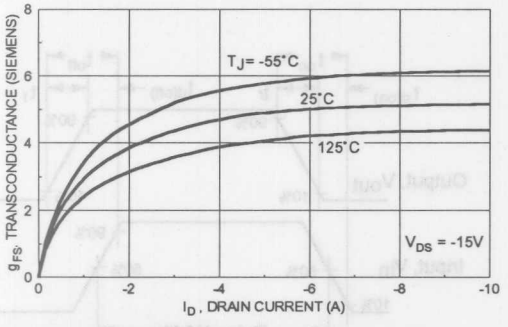


Figure 22. P-Channel Transconductance Variation with Drain Current and Temperature.

Typical Electrical Characteristic: N & P-Channel (continued)

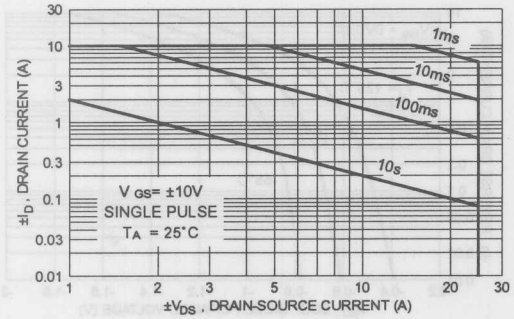


Figure 23. Maximum Safe Operating Area for both N & P-Channel.

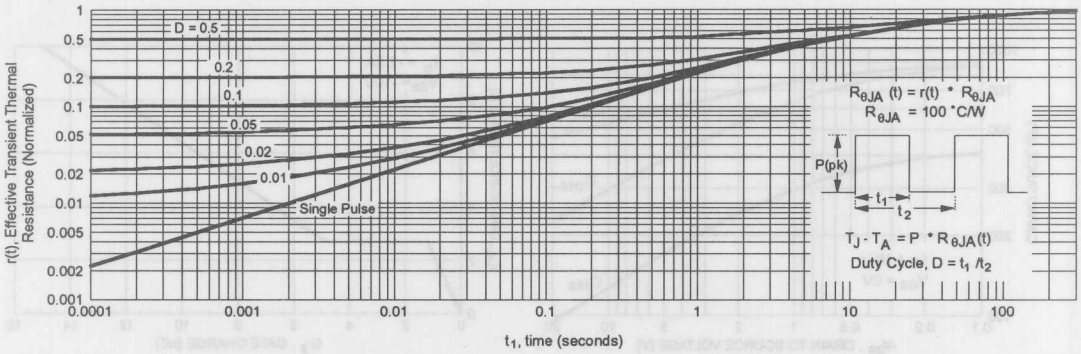


Figure 24. Transient Thermal Response Curve for N or P-Channel Surface-Mounted Device.

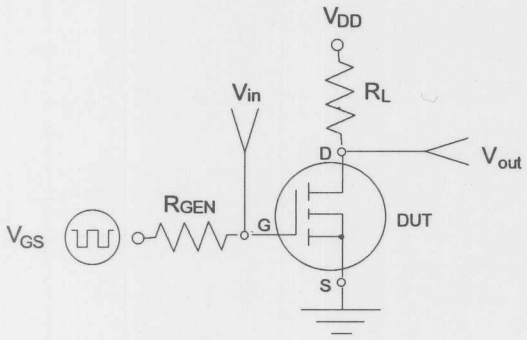


Figure 25. N or P-Channel Switching Test Circuit.

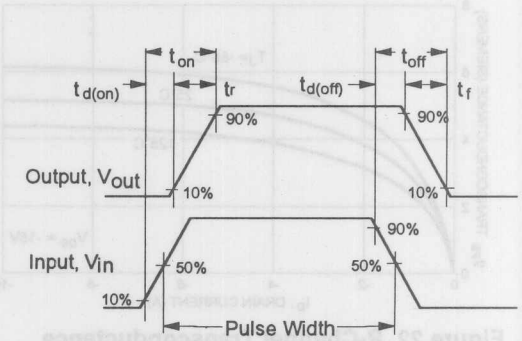


Figure 26. N or P-Channel Switching Waveforms.

National Semiconductor

August 1993

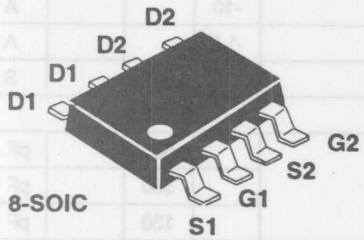
NDS9953
Dual P-Channel Enhancement Mode Field Effect Transistor

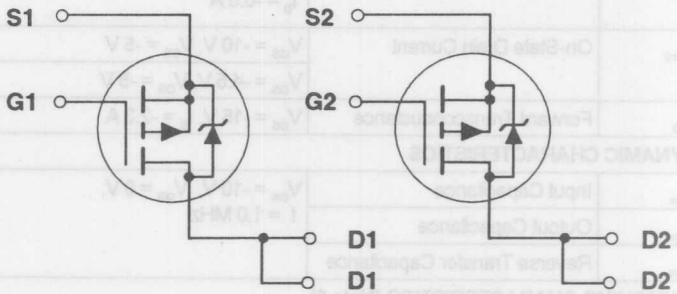
General Description

These P-channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulses in the avalanche and commutation modes. These devices are particularly suited for low voltage applications such as laptop computer power management and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- 2.3A, -20V. $R_{DS(ON)}$ = 0.25Ω.
- Rugged internal source-drain diode can eliminate the need for an external Zener diode transient suppressor.
- High density cell design (3.8 million/in²) for extremely low $R_{DS(ON)}$.
- High power and current handling capability in a widely used surface mount package.
- Dual MOSFET in surface mount package.
- Critical DC electrical parameters specified at elevated temperature.





Absolute Maximum Ratings

T_C = 25°C unless otherwise noted

Symbol	Parameter	NDS9953	Units
V_{DSS}	Drain-Source Voltage	-20	V
V_{DGR}	Drain-Gate Voltage (R_{GS} ≤ 1 MΩ)	-20	V
V_{GSS}	Gate-Source Voltage	± 20	V
I_D	Drain Current - Continuous T_A = 25°C	± 2.3	A
	- Pulsed	± 10	A
	- Continuous T_A = 70°C	± 1.8	A
P_D	Maximum Power Dissipation T_A = 25°C	2 (Note 1)	W
	T_A = 70°C	1.3 (Note 1)	W
T_J,T_{STG}	Operating and Storage Temperature Range	-55 to 150	°C
THERMAL CHARACTERISTICS			
$R_{\theta JA}(t)$	Thermal Resistance, Junction-to-Ambient (Surface Mounted. Pulse time = 10 seconds)	62.5 (Note 1)	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Surface Mounted. Steady-State)	100	°C/W

Electrical Characteristics (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = -250 µA	-20			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -16 V, V_{GS} = 0 V			-2	µA
		T_C = 55°C			-25	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = -250 µA	-1	-2	-3	V
		T_C=125°C	-0.85	-1.7	-2.6	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = -10 V, I_D = -1A		0.18	0.25	Ω
		T_C=125°C		0.24	0.35	Ω
		V_{GS} = -4.5 V, I_D = -0.5 A		0.26	0.4	Ω
		T_C=125°C		0.35	0.56	Ω
$I_{D(on)}$	On-State Drain Current	V_{GS} = -10 V, V_{DS} = -5 V	-10			A
		V_{GS} = -4.5 V, V_{DS} = -5 V	-1.5			A
g_{FS}	Forward Transconductance	V_{DS} = -15 V, I_D = -2.3 A		3.8		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = -10 V, V_{GS} = 0 V, f = 1.0 MHz		525		pF
C_{oss}	Output Capacitance			300		pF
C_{rss}	Reverse Transfer Capacitance			130		pF
SWITCHING CHARACTERISTICS (Note 2)						
$t_{D(ON)}$	Turn - On Delay Time	V_{DD} = -10 V, I_D = -1 A, V_{GEN} = -10 V, R_{GEN} = 6 Ω		8	40	ns
t_r	Turn - On Rise Time			15	40	ns
$t_{D(OFF)}$	Turn - Off Delay Time			25	90	ns
t_f	Turn - Off Fall Time			8	50	ns
Q_g	Total Gate Charge	V_{DS} = -10 V, I_D = -2.3 A, V_{GS} = -10 V		15	25	nC
Q_{gs}	Gate-Source Charge			1.2		nC
Q_{gd}	Gate-Drain Charge			4.8		nC
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain-Source Diode Forward Current				-1.6	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = -1.25 A (Note 2)		-0.94	-1.6	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0V, I_S = 1.25 A, dI_S/dt = 100 A/µs		29	100	ns
I_{rr}	Reverse Recovery Current			1.9		A

Notes:

1. Power dissipation and thermal resistance determinations based on an assumption that a 10 second pulse is equivalent to steady-state.
2. Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

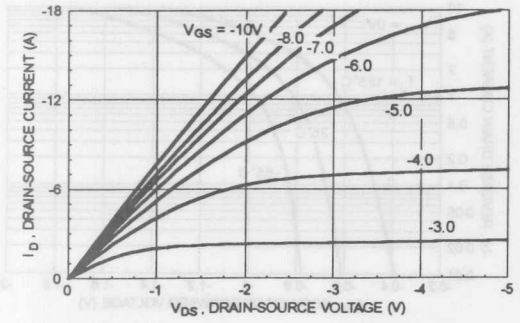


Figure 1. On-Region Characteristics.

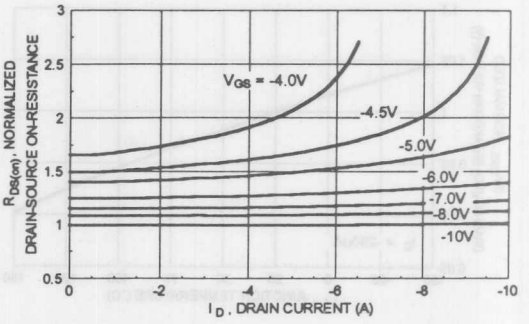


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current.

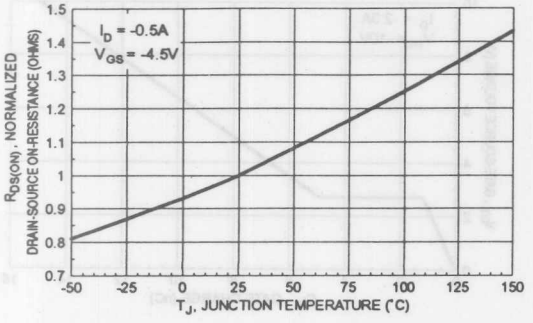


Figure 3. On-Resistance Variation with Temperature.

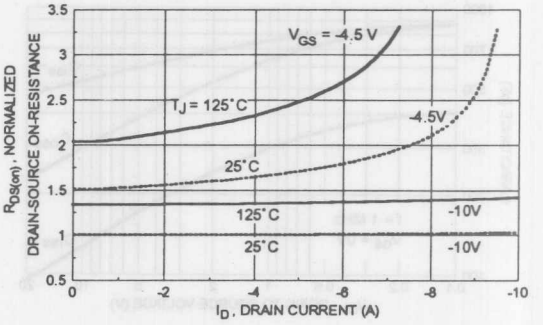


Figure 4. On-Resistance Variation with Drain Current and Temperature.

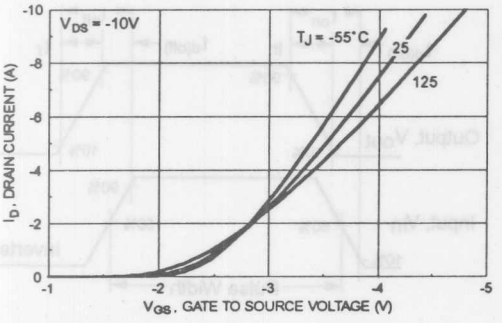


Figure 5. Drain Current Variation with Gate Voltage and Temperature.

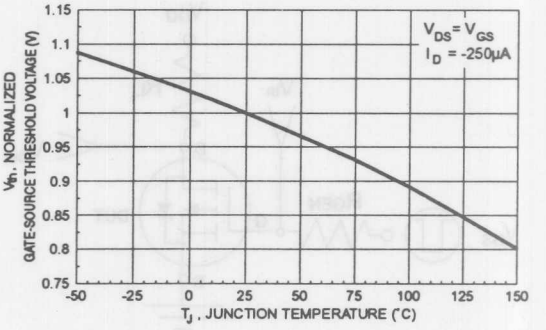


Figure 6. Gate Threshold Variation with Temperature.

Typical Electrical Characteristics (continued)

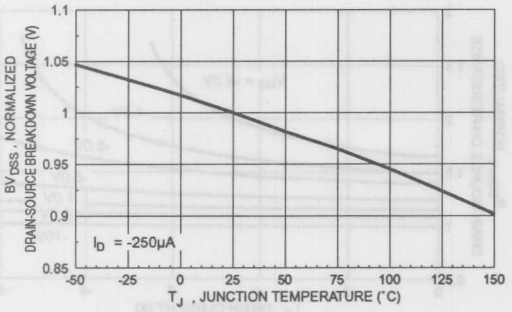


Figure 7. Breakdown Voltage Variation with Temperature.

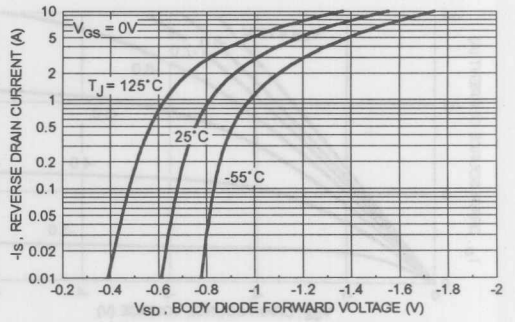


Figure 8. Body Diode Forward Voltage Variation with Current and Temperature

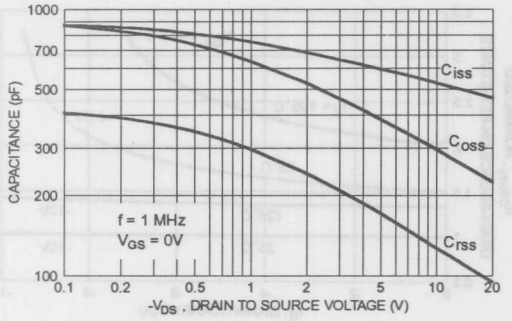


Figure 9. Capacitance Characteristics.

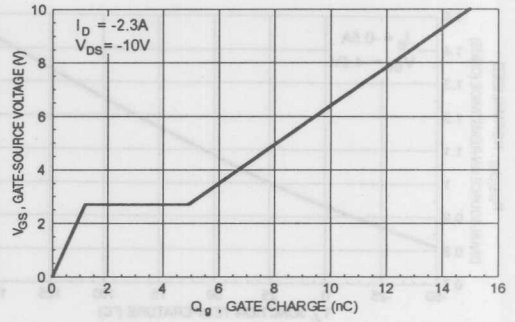


Figure 10. Gate Charge Characteristics.

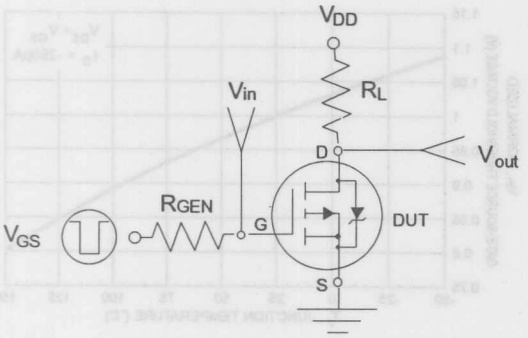


Figure 11. Switching Test Circuit

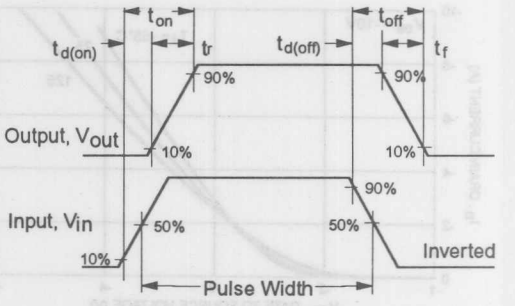


Figure 12. Switching Waveforms

Typical Electrical Characteristics (continued)

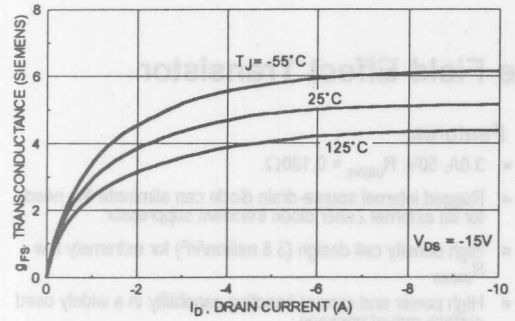


Figure 13. Transconductance Variation with Drain Current and Temperature.

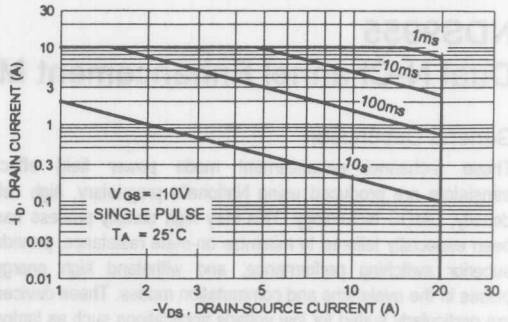


Figure 14. Maximum Safe Operating Area.

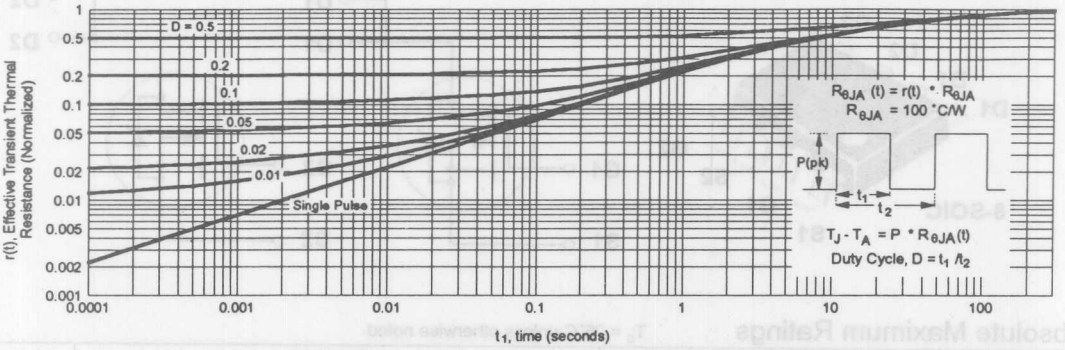


Figure 15. Transient Thermal Response Curve.

National Semiconductor

May 1993

NDS9955

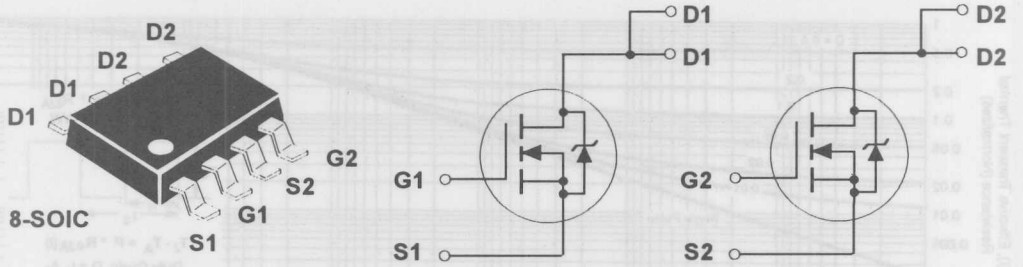
Dual N-Channel Enhancement Mode Field Effect Transistor

General Description

These n-channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulses in the avalanche and commutation modes. These devices are particularly suited for low voltage applications such as laptop computer power management and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- 3.0A, 50V. $R_{DS(ON)}$ = 0.130Ω.
- Rugged internal source-drain diode can eliminate the need for an external Zener diode transient suppressor.
- High density cell design (3.8 million/in²) for extremely low $R_{DS(ON)}$.
- HIgh power and current handling capability in a widely used surface mount package.
- Dual MOSFET in surface mount package.
- Critical DC electrical parameters specified at elevated temperature.



Absolute Maximum Ratings

T_C = 25°C unless otherwise noted

Symbol	Parameter	NDS9955	Units
V_{DSS}	Drain-Source Voltage	50	V
V_{DGR}	Drain-Gate Voltage ($R_{GS} \leq 1$ MΩ)	50	V
V_{GSS}	Gate-Source Voltage	± 20	V
I_D	Drain Current - Continuous @ T_A = 25°C	± 3	A
	- Continuous @ T_A = 70°C	± 2.3	A
	- Pulsed	± 10	A
P_D	Maximum Power Dissipation @ T_A = 25°C	2 (Note 1)	W
T_J,T_{STG}	Operating and Storage Temperature Range	-55 to 150	°C
THERMAL CHARACTERISTICS			
$R_{\theta JA}(t)$	Thermal Resistance, Junction-to-Ambient (Surface Mounted. Pulse time = 10 seconds)	62.5 (Note 1)	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Surface Mounted. Steady-State)	100	°C/W

Electrical Characteristics (T_c = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	50			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 40 V, V_{GS} = 0 V			2	µA
		V_{DS} = 40 V, V_{GS} = 0 V, T_c = 55°C			25	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	1	1.5	3	V
		V_{DS} = V_{GS}, I_D = 250 µA, T_c=125°C	0.7		2.2	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 3.0 A		0.084	0.13	Ω
		V_{GS} = 10 V, I_D = 3.0 A, T_c=125°C		0.13	0.2	Ω
		V_{GS} = 4.5 V, I_D = 1.5 A		0.11	0.2	Ω
		V_{GS} = 4.5 V, I_D = 1.5 A, T_c=125°C		0.17	0.3	Ω
$I_{D(on)}$	On-State Drain Current	V_{GS} = 10 V, V_{DS} = 10 V	10			A
		V_{GS} = 4.5 V, V_{DS} = 10 V	3.5			A
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 3.0 A	4	6		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz		435		pF
C_{oss}	Output Capacitance			120		pF
C_{rss}	Reverse Transfer Capacitance			30		pF
SWITCHING CHARACTERISTICS (Note 2)						
$t_{D(ON)}$	Turn - On Delay Time	V_{DD} = 25V, I_D = 1 A, V_{GS} = 10 V, R_{GEN} = 6 Ω		8	20	ns
t_r	Turn - On Rise Time			4	20	ns
$t_{D(OFF)}$	Turn - Off Delay Time			24	70	ns
t_f	Turn - Off Fall Time			7	50	ns
Q_g	Total Gate Charge	V_{DS} = 25 V, I_D = 2 A, V_{GS} = 10 V		13	30	nC
Q_{gs}	Gate-Source Charge			0.8		nC
Q_{gd}	Gate-Drain Charge			4.2		nC
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain-Source Diode Forward Current				2	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 1.5 A (Note 2)		0.8	1.2	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0V, I_S = 1.5 A, dI_S/dt = 100 A/µs		52	100	ns
I_{rr}	Reverse Recovery Current			2.3		A

Notes:

1. Power dissipation and thermal resistance determinations based on an assumption that a 10 second pulse is equivalent to steady-state.
2. Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

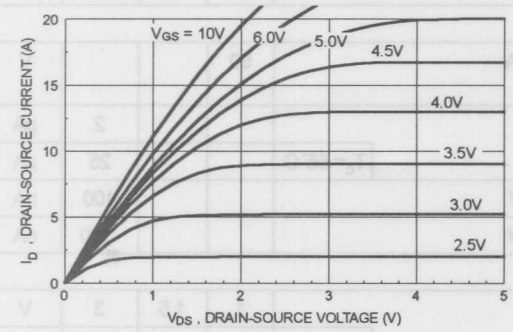


Figure 1. On-Region Characteristics.

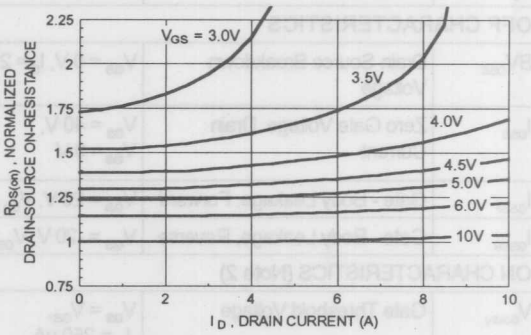


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current.

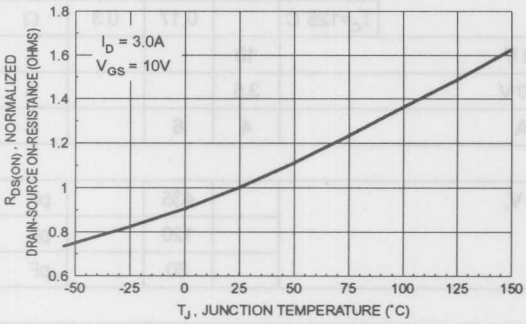


Figure 3. On-Resistance Variation with Temperature.

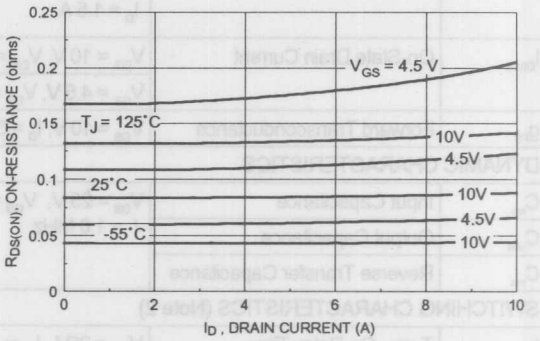


Figure 4. On-Resistance Variation with Drain Current and Temperature.

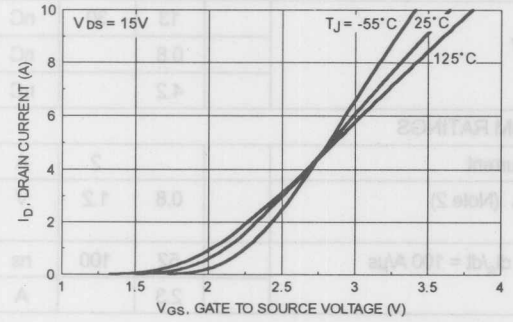


Figure 5. Drain Current Variation with Gate Voltage and Temperature.

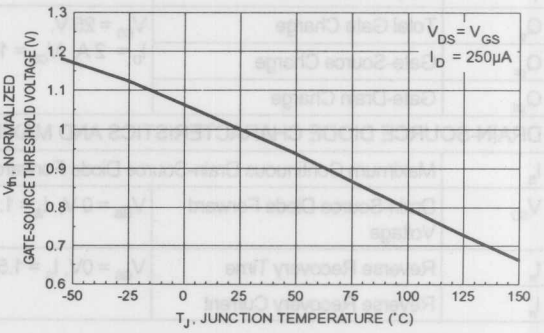


Figure 6. Gate Threshold Variation with Temperature.

Typical Electrical Characteristics (continued)

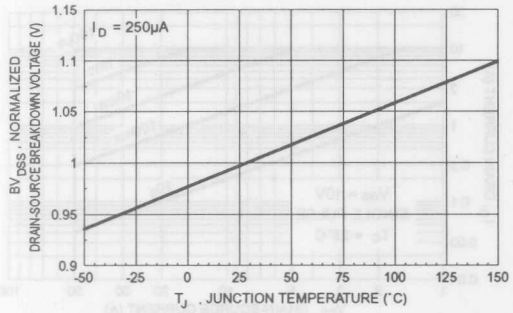


Figure 7. Breakdown Voltage Variation with Temperature.

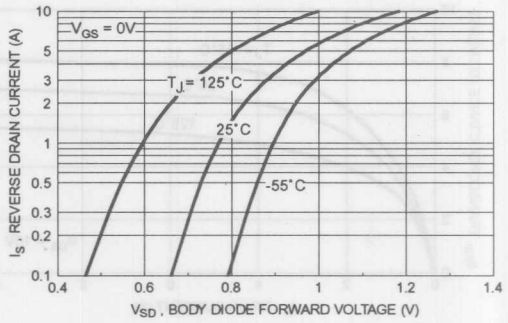


Figure 8. Body Diode Forward Voltage Variation with Current and Temperature

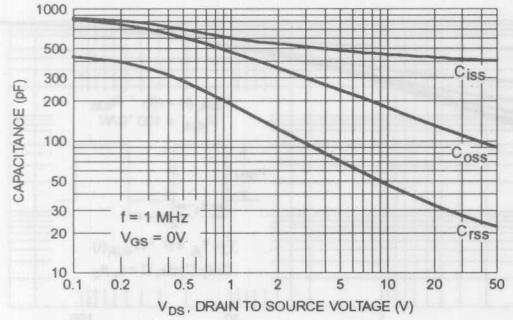


Figure 9. Capacitance Characteristics.

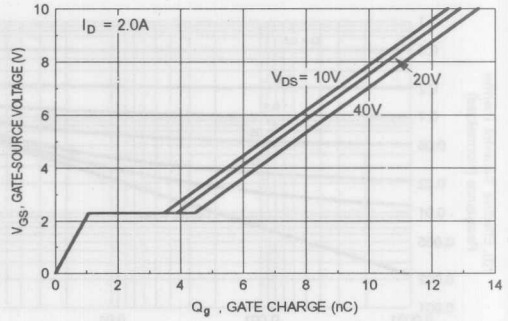


Figure 10. Gate Charge Characteristics.

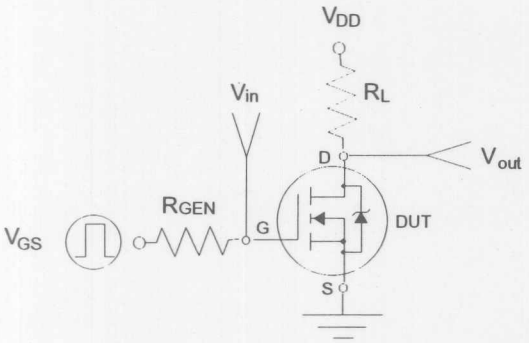


Figure 11. Switching Test Circuit

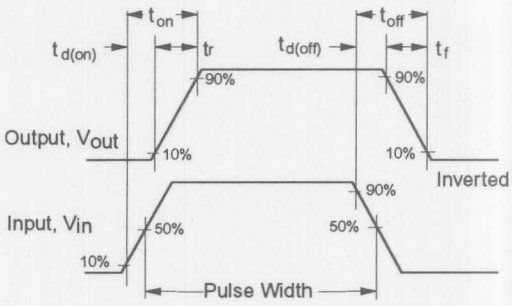


Figure 12. Switching Waveforms

Typical Electrical Characteristics (continued)

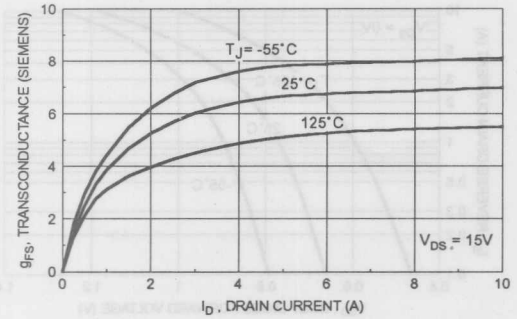


Figure 13. Transconductance Variation with Drain Current and Temperature.

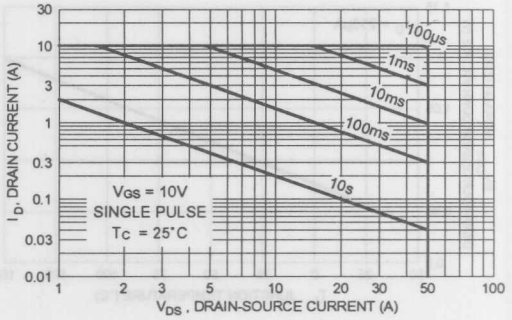


Figure 14. Maximum Safe Operating Area.

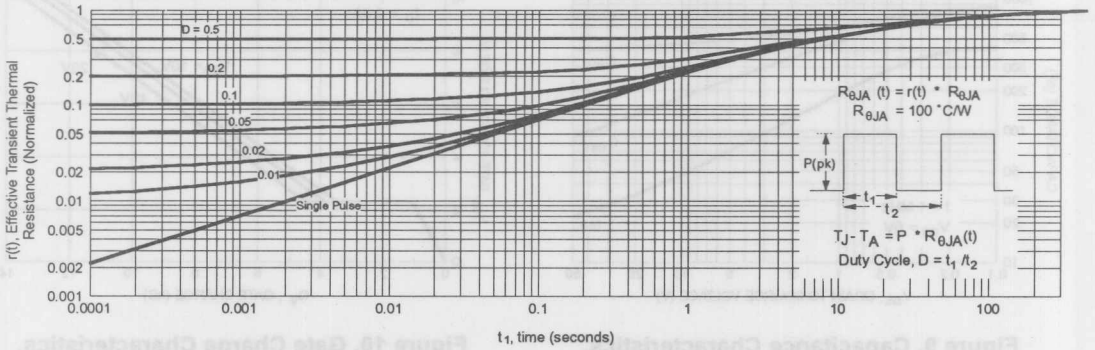


Figure 15. Transient Thermal Response Curve.

National Semiconductor

July 1993

NDS9956

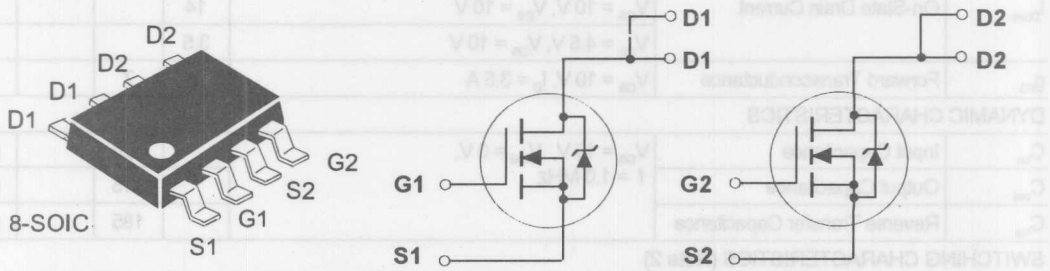
Dual N-Channel Enhancement Mode Field Effect Transistor

General Description

These n-channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulses in the avalanche and commutation modes. These devices are particularly suited for low voltage applications such as laptop computer power management and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- 3.5A, 20V. $R_{DS(ON)}$ = 0.10Ω.
- Rugged internal source-drain diode can eliminate the need for an external Zener diode transient suppressor.
- High density cell design (3.8 million/in²) for extremely low $R_{DS(ON)}$.
- High power and current handling capability in a widely used surface mount package.
- Dual MOSFET in surface mount package
- Critical DC electrical parameters specified at elevated temperature



Absolute Maximum Ratings

T_C = 25°C unless otherwise noted

Symbol	Parameter	NDS9956	Units
V_{DSS}	Drain-Source Voltage	20	V
V_{DGR}	Drain-Gate Voltage ($R_{GS} \leq 1$ MΩ)	20	V
V_{GSS}	Gate-Source Voltage	± 20	V
I_D	Drain Current - Continuous @ T_A = 25°C	± 3.5	A
	- Continuous @ T_A = 70°C	± 2.8	A
	- Pulsed	± 14	A
P_D	Total Power Dissipation @ T_C = 25°C	2 (Note 1)	W
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to 150	°C
THERMAL CHARACTERISTICS			
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Surface Mounted. Pulse time = 10 seconds)	62.5 (Note 1)	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Surface Mounted. Steady-State)	100	°C/W

Electrical Characteristics (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	20			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 16 V, V_{GS} = 0 V			2	µA
		V_{DS} = 16 V, V_{GS} = 0 V, T_C = 55°C			25	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	1		3	V
		V_{DS} = V_{GS}, I_D = 250 µA, T_C=125°C	0.7		2.2	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 2.2 A		0.062	0.1	Ω
		V_{GS} = 10 V, I_D = 2.2 A, T_C=125°C		0.085	0.2	Ω
		V_{GS} = 4.5 V, I_D = 1 A		0.08	0.2	Ω
		V_{GS} = 4.5 V, I_D = 1 A, T_C=125°C		0.11	0.4	Ω
$I_{D(on)}$	On-State Drain Current	V_{GS} = 10 V, V_{DS} = 10 V	14			A
		V_{GS} = 4.5 V, V_{DS} = 10 V	3.5			A
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 3.5 A	3	7		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 10 V, V_{GS} = 0 V, f = 1.0 MHz		525		pF
C_{oss}	Output Capacitance			315		pF
C_{rss}	Reverse Transfer Capacitance			185		pF
SWITCHING CHARACTERISTICS (Note 2)						
$t_{D(ON)}$	Turn - On Delay Time	V_{DD} = 10V, I_D = 1 A, V_{GS} = 10 V, R_{GEN} = 6 Ω		6	20	ns
t_r	Turn - On Rise Time			12	20	ns
$t_{D(OFF)}$	Turn - Off Delay Time			22	90	ns
t_f	Turn - Off Fall Time			8	50	ns
Q_g	Total Gate Charge	V_{DS} = 10 V, I_D = 1.8 A, V_{GS} = 10 V		17	30	nC
Q_{gs}	Gate-Source Charge			1.2		nC
Q_{gd}	Gate-Drain Charge			5		nC
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuos Drain-Source Diode Forward Current				1.7	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 1.25 A (Note 2)		0.78	1.4	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0V, I_S = 1.25 A, dI_S/dt = 100 A/µs		70	100	ns

Notes:

1. Power dissipation and thermal resistance determinations based on an assumption that a 10 second pulse is equivalent to steady-state.
2. Pulse Test: Pulse Width ≤ 300 ms, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

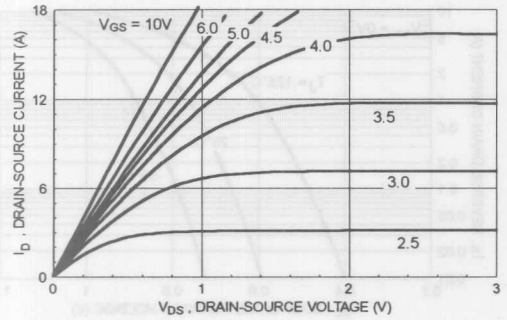


Figure 1. On-Region Characteristics.

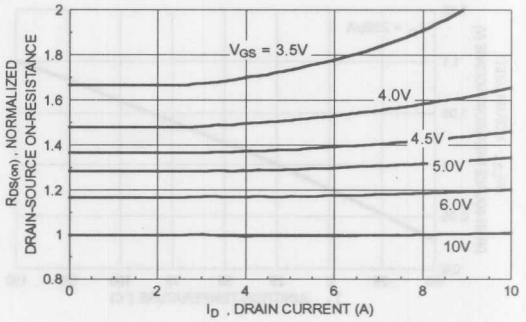


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current.

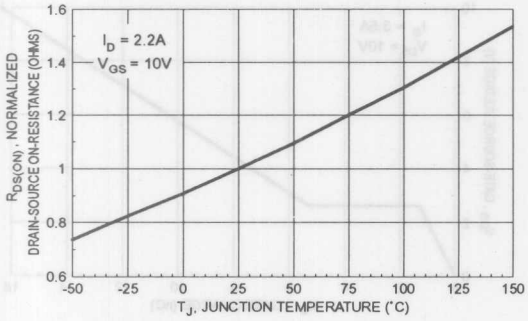


Figure 3. On-Resistance Variation with Temperature.

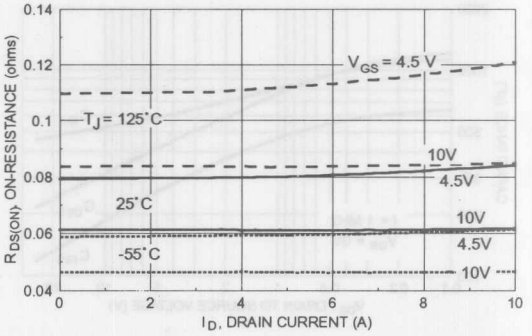


Figure 4. On-Resistance Variation with Drain Current and Temperature.

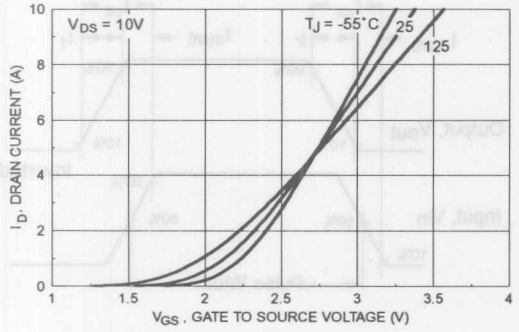


Figure 5. Transfer Characteristics.

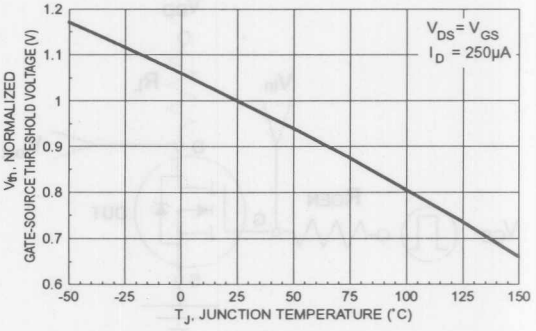


Figure 6. Gate Threshold Variation with Temperature.

Typical Electrical Characteristics (continued)

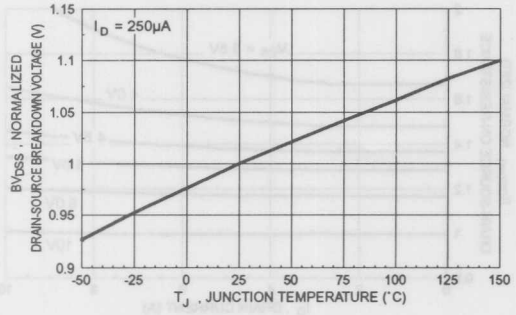


Figure 7. Breakdown Voltage Variation with Temperature.

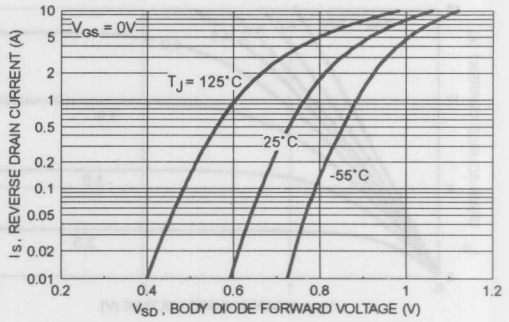


Figure 8. Body Diode Forward Voltage Variation with Current and Temperature

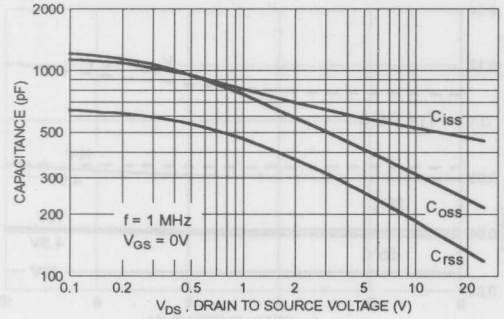


Figure 9. Capacitance Characteristics.

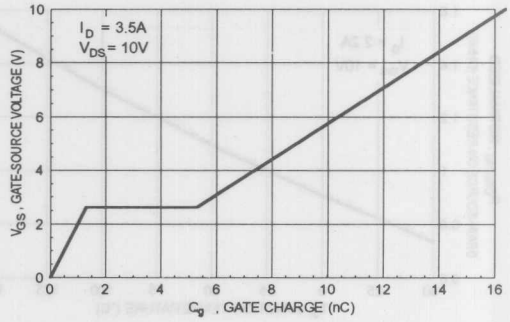


Figure 10. Gate Charge Characteristics.

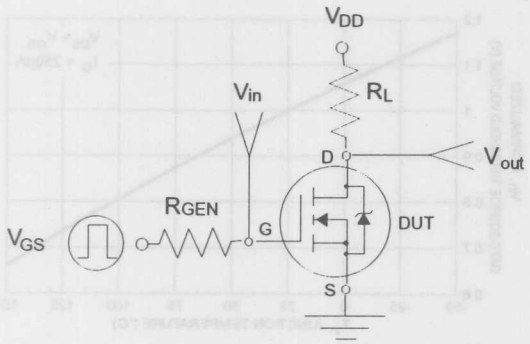


Figure 11. Switching Test Circuit

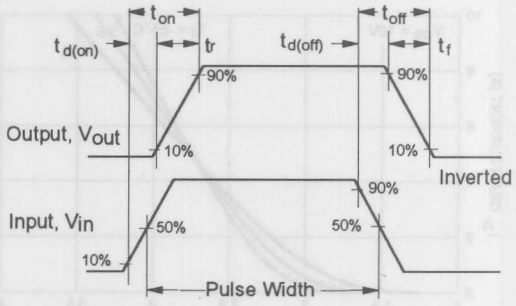


Figure 12. Switching Waveforms

Typical Electrical Characteristics (continued)

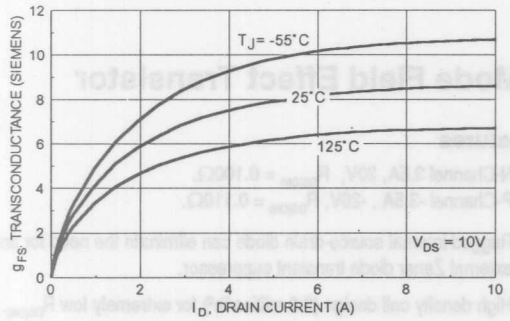


Figure 13. Transconductance Variation

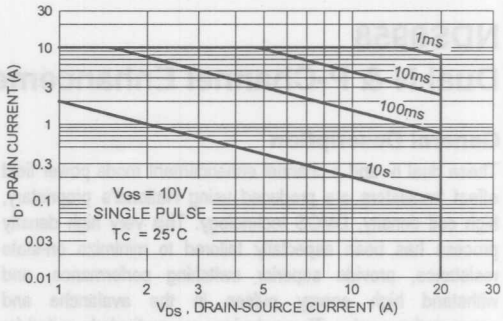


Figure 14. Maximum Safe Operating Area.

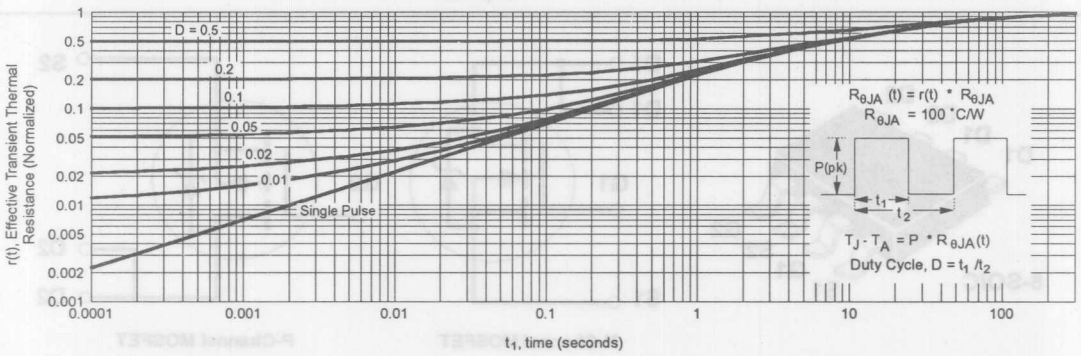


Figure 15. Transient Thermal Response Curve for Surface-Mounted Device.

National Semiconductor

July 1993

ADVANCE INFORMATION

NDS9958

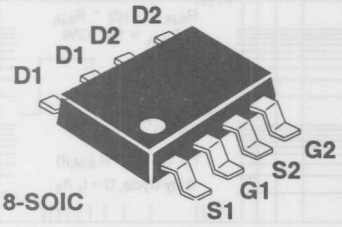
Dual N & P-Channel Enhancement Mode Field Effect Transistor

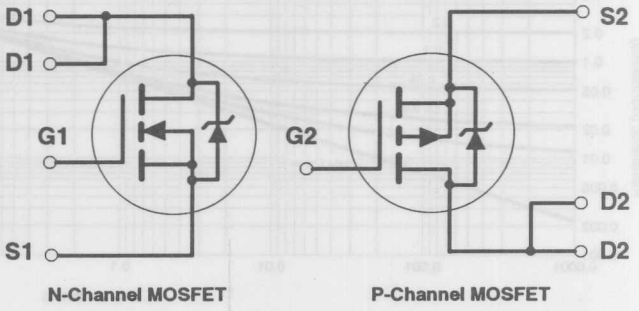
General Description

These dual n- and p-channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulses in the avalanche and commutation modes. These devices are particularly suited for low voltage applications such as laptop computer power management and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- N-Channel 3.5A, 20V, $R_{DS(ON)}$ = 0.100Ω.
  P-Channel -3.5A , -20V, $R_{DS(ON)}$ = 0.110Ω.
- Rugged internal source-drain diode can eliminate the need for an external Zener diode transient suppressor.
- High density cell design (3.8 million/in²) for extremely low $R_{DS(ON)}$.
- High power and current handling capability in a widely used surface mount package.
- Dual (N & P-Channel) MOSFET in surface mount package.
- Critical DC electrical parameters specified at elevated temperature.





Absolute Maximum Ratings

T_C = 25°C unless otherwise noted

Symbol	Parameter	N-Channel	P-Channel	Units
V_{DSS}	Drain-Source Voltage	20	-20	V
V_{DGR}	Drain-Gate Voltage ($R_{GS} \leq 1$ MΩ)	20	-20	V
V_{GSS}	Gate-Source Voltage	± 20	± 20	V
I_D	Drain Current - Continuous @ T_A = 25°C	± 3.5	± 3.5	A
	- Continuous @ T_A = 70°C	± 2.8	± 2.8	A
	- Pulsed	± 14	± 14	A
P_D	Maximum Power Dissipation @ T_A = 25°C	2 (Note 1)		W
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to 150		°C
THERMAL CHARACTERISTICS				
$R_{\theta JA}(t)$	Thermal Resistance, Junction-to-Ambient (Surface Mounted. Pulse time = 10 seconds)	62.5 (Note 1)		°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Surface Mounted. Steady-State)	100		°C/W

Electrical Characteristics (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Type	Min	Typ	Max	Units
OFF CHARACTERISTICS							
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	N-Ch	20			V
		V_{GS} = 0 V, I_D = -250 µA	P-Ch	-20			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 16 V, V_{GS} = 0 V	N-Ch			1	µA
		V_{DS} = 16 V, V_{GS} = 0 V, T_C = 55°C	N-Ch			10	µA
		V_{DS} = -16 V, V_{GS} = 0 V	P-Ch			-1	µA
		V_{DS} = -16 V, V_{GS} = 0 V, T_C = 55°C	P-Ch			-10	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V				100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS} = 0 V				-100	nA
ON CHARACTERISTICS (Note 2)							
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	N-Ch	1	1.5	3	V
		V_{DS} = V_{GS}, I_D = 250 µA, T_C=125°C	N-Ch	0.7	1.1	2.2	V
		V_{DS} = V_{GS}, I_D = -250 µA	P-Ch	-1		-3	V
		V_{DS} = V_{GS}, I_D = -250 µA, T_C=125°C	P-Ch	TBD		TBD	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 3.5 A	N-Ch		0.062	0.100	Ω
		V_{GS} = 10 V, I_D = 3.5 A, T_C=125°C	N-Ch		0.085	0.14	Ω
		V_{GS} = 6V, I_D = 3.0 A	N-Ch		0.073	0.12	Ω
		V_{GS} = 4.5 V, I_D = 1.0 A	N-Ch		0.08	0.15	Ω
		V_{GS} = 4.5 V, I_D = 1.0 A, T_C=125°C	N-Ch		0.11	0.21	Ω
		V_{GS} = -10 V, I_D = -3.5 A	P-Ch			0.11	Ω
		V_{GS} = -10 V, I_D = -3.5 A, T_C=125°C	P-Ch			TBD	Ω
		V_{GS} = -6V, I_D = -3.0 A	P-Ch			0.12	Ω
		V_{GS} = -4.5 V, I_D = -1.0 A	P-Ch			0.19	Ω
		V_{GS} = -4.5 V, I_D = -1.0 A, T_C=125°C	P-Ch			TBD	Ω
$I_{D(on)}$	On-State Drain Current	V_{GS} = 10 V, V_{DS} = 5 V	N-Ch	14			A
		V_{GS} = -10 V, V_{DS} = -5 V	P-Ch	-14			A
		V_{GS} = 4.5 V, V_{DS} = 5 V	N-Ch	3.5			A
		V_{GS} = -4.5 V, V_{DS} = -5 V	P-Ch	-2.5			A
g_{FS}	Forward Transconductance	V_{DS} = 15 V, I_D = 3.5 A	N-Ch		7		S
		V_{DS} = -15 V, I_D = -3.5 A	P-Ch		TBD		S
DYNAMIC CHARACTERISTICS							
C_{iss}	Input Capacitance	N-Channel V_{DS} = 10V, V_{GS} = 0 V, f = 1.0 MHz	N-Ch		525		pF
			P-Ch		TBD		pF
C_{oss}	Output Capacitance		N-Ch		315		pF
		P-Channel V_{DS} = -10 V, V_{GS} = 0 V, f = 1.0 MHz	P-Ch		TBD		pF
C_{rss}	Reverse Transfer Capacitance		N-Ch		185		pF
			P-Ch		TBD		pF

Electrical Characteristics (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Type	Min	Typ	Max	Units
SWITCHING CHARACTERISTICS (Note 2)							
$t_{D(ON)}$	Turn - On Delay Time	N-Channel V_{DD} = 10 V, I_D = 1 A, V_{GEN} = 10 V, R_{GEN} = 6 Ω P-Channel V_{DD} = -10 V, I_D = -1 A, V_{GEN} = -10 V, R_{GEN} = 6 Ω	N-Ch		6		ns
			P-Ch		TBD		ns
t_r	Turn - On Rise Time		N-Ch		12		ns
			P-Ch		TBD		ns
$t_{D(OFF)}$	Turn - Off Delay Time		N-Ch		22		ns
			P-Ch		TBD		ns
t_f	Turn - Off Fall Time		N-Ch		8		ns
			P-Ch		TBD		ns
Q_g	Total Gate Charge	N-Channel V_{DS} = 10V, I_D = 3.5A, V_{GS} = 10 V P-Channel V_{DS} = -10V, I_D = -3.5A, V_{GS} = -10 V	N-Ch		17		nC
			P-Ch		TBD		nC
Q_{gs}	Gate-Source Charge		N-Ch		1.2		nC
			P-Ch		TBD		nC
Q_{gd}	Gate-Drain Charge		N-Ch		5		nC
			P-Ch		TBD		nC
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS							
I_S	Maximum Continuous Drain-Source Diode Forward Current		N-Ch			1.7	A
			P-Ch			-1.7	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 3.5 A (Note 2)	N-Ch		0.86	1.2	V
		V_{GS} = 0 V, I_S = -3.5A (Note 2)	P-Ch			-1.2	V
t_{rr}	Reverse Recovery Time	N-Channel V_{GS} = 0V, I_S = 3.5 A, dI_S/dt = 100 A/µs	N-Ch			100	ns
			P-Ch			100	ns
I_{rr}	Reverse Recovery Current	P-Channel V_{GS} = 0V, I_S = -3.5 A, dI_S/dt = 100 A/µs	N-Ch		TBD		A
			P-Ch		TBD		A

Notes:
1. Power dissipation and thermal resistance determinations based on an assumption that a 10 second pulse is equivalent to steady-state.
2. Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics: N-Channel

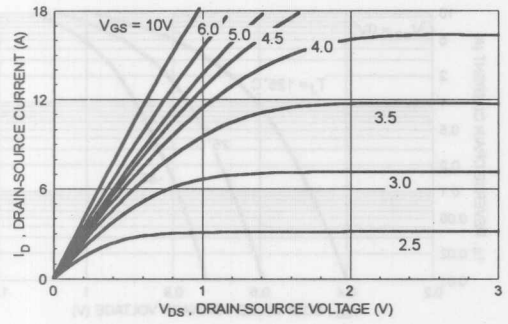


Figure 1. On-Region Characteristics.

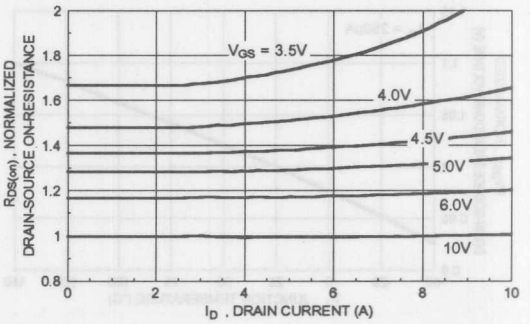


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current.

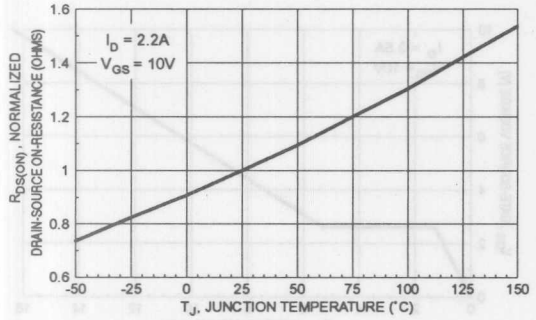


Figure 3. On-Resistance Variation with Temperature.

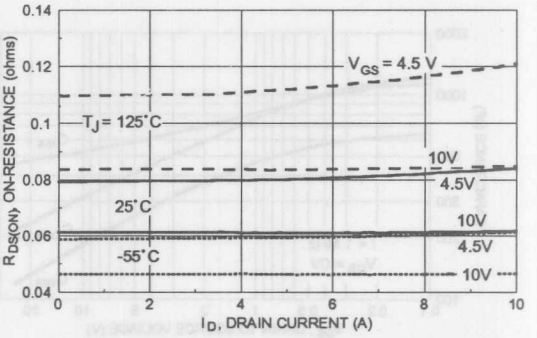


Figure 4. On-Resistance Variation with Drain Current and Temperature.

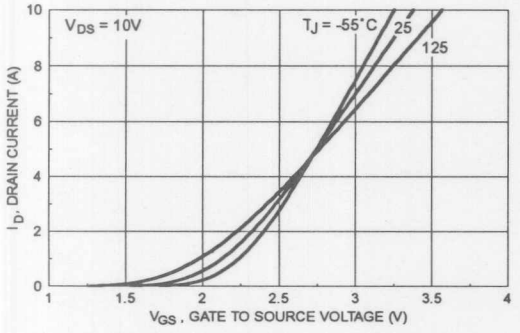


Figure 5. Transfer Characteristics.

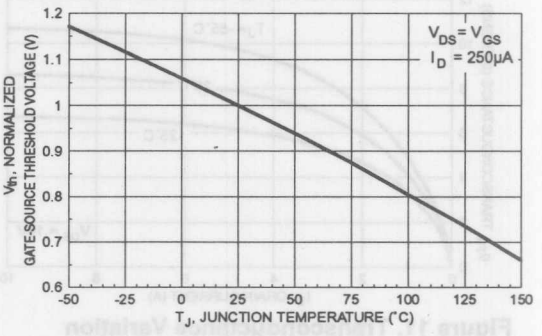


Figure 6. Gate Threshold Variation with Temperature.

Typical Electrical Characteristics: N-Channel (continued)

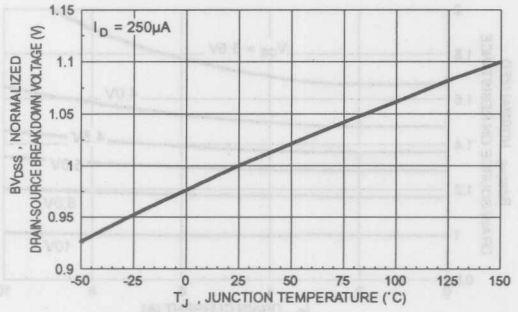


Figure 7. Breakdown Voltage Variation with Temperature.

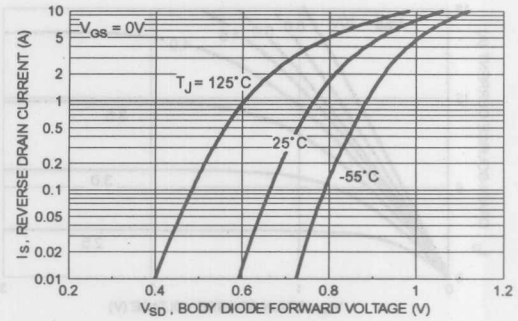


Figure 8. Body Diode Forward Voltage Variation with Current and Temperature

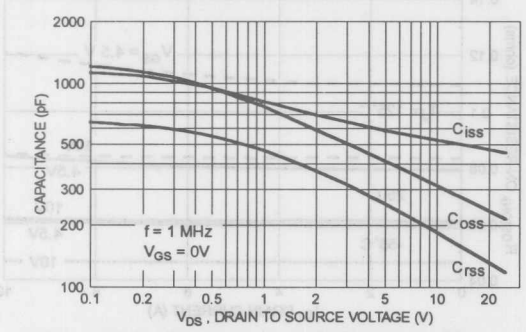


Figure 9. Capacitance Characteristics.

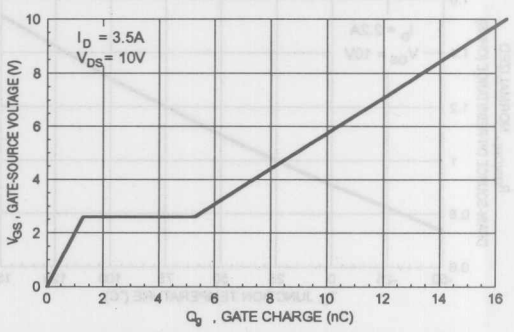


Figure 10. Gate Charge Characteristics.

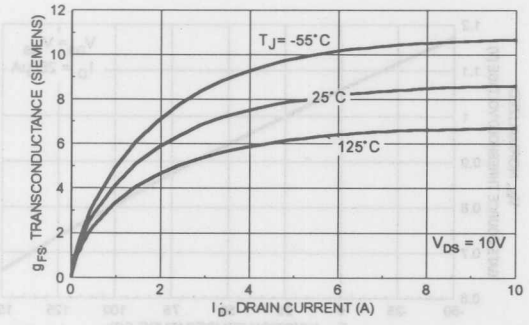


Figure 11. Transconductance Variation with Drain Current and Temperature.

Typical Electrical Characteristic: N & P-Channel (continued)

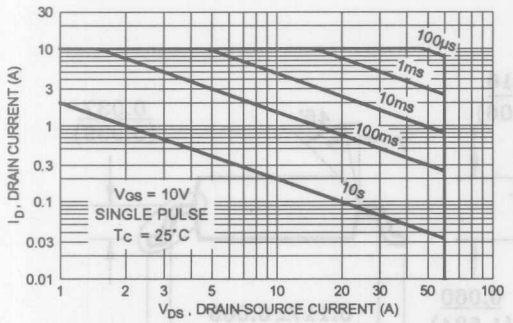


Figure 12. Maximum Safe Operating Area.

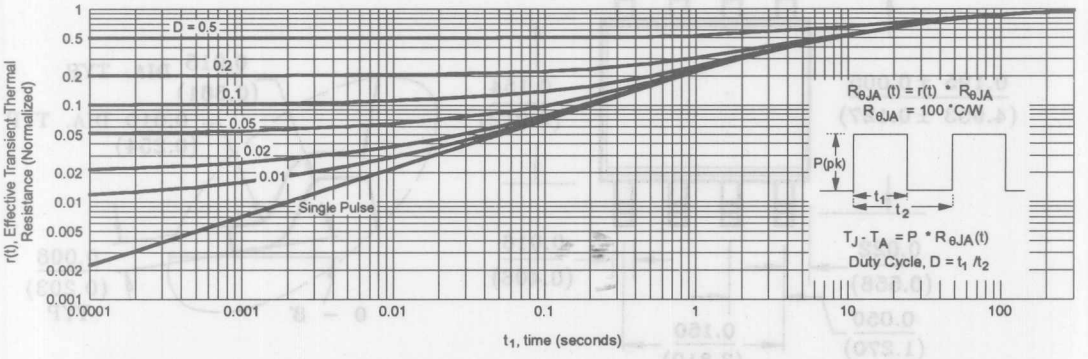


Figure 13. Transient Thermal Response Curve for Surface-Mounted Device.

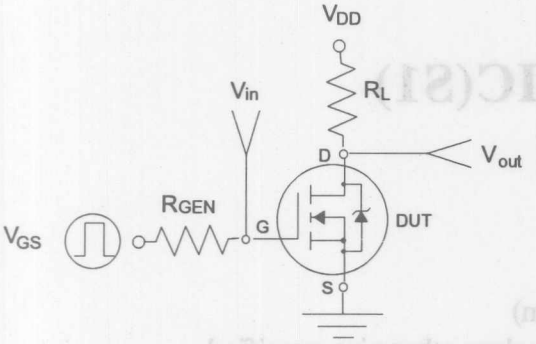


Figure 14. Switching Test Circuit

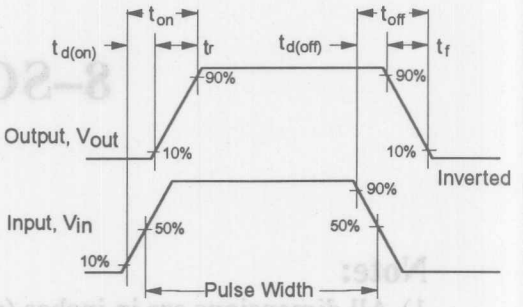
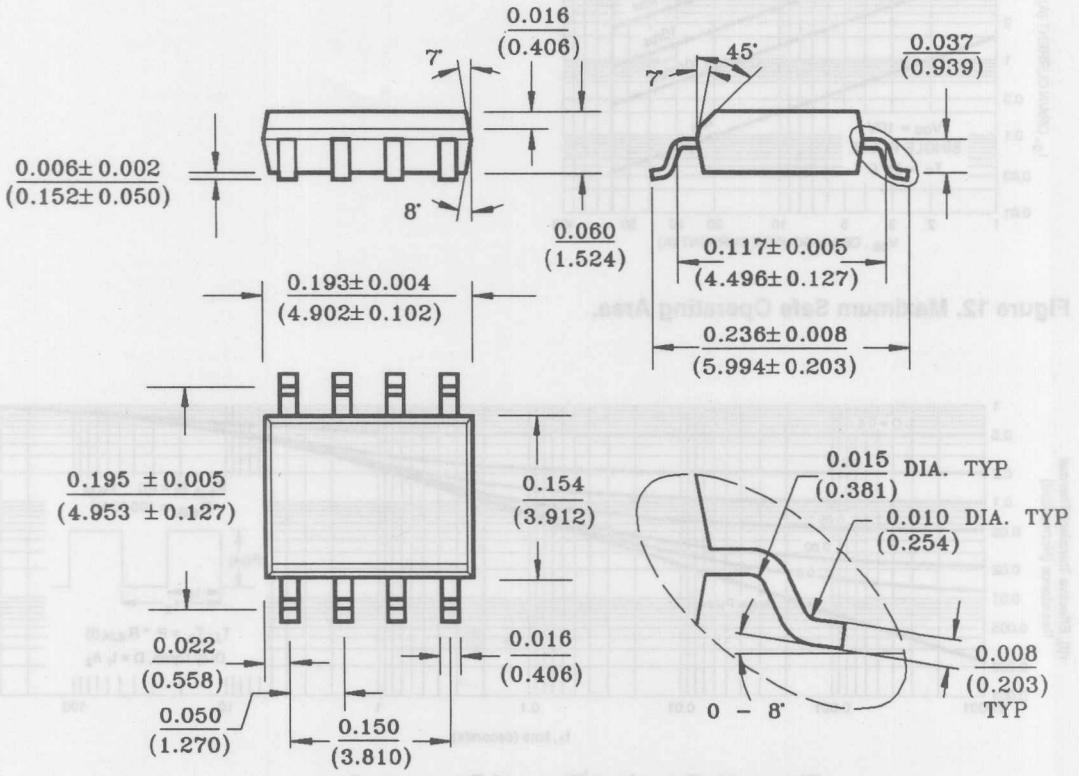


Figure 15. Switching Waveforms



8–SOIC(S1)

Note:

1) All dimensions are in inches (mm)

2) Gen tolerance ± 0.002 (0.0508) unless otherwise specified.